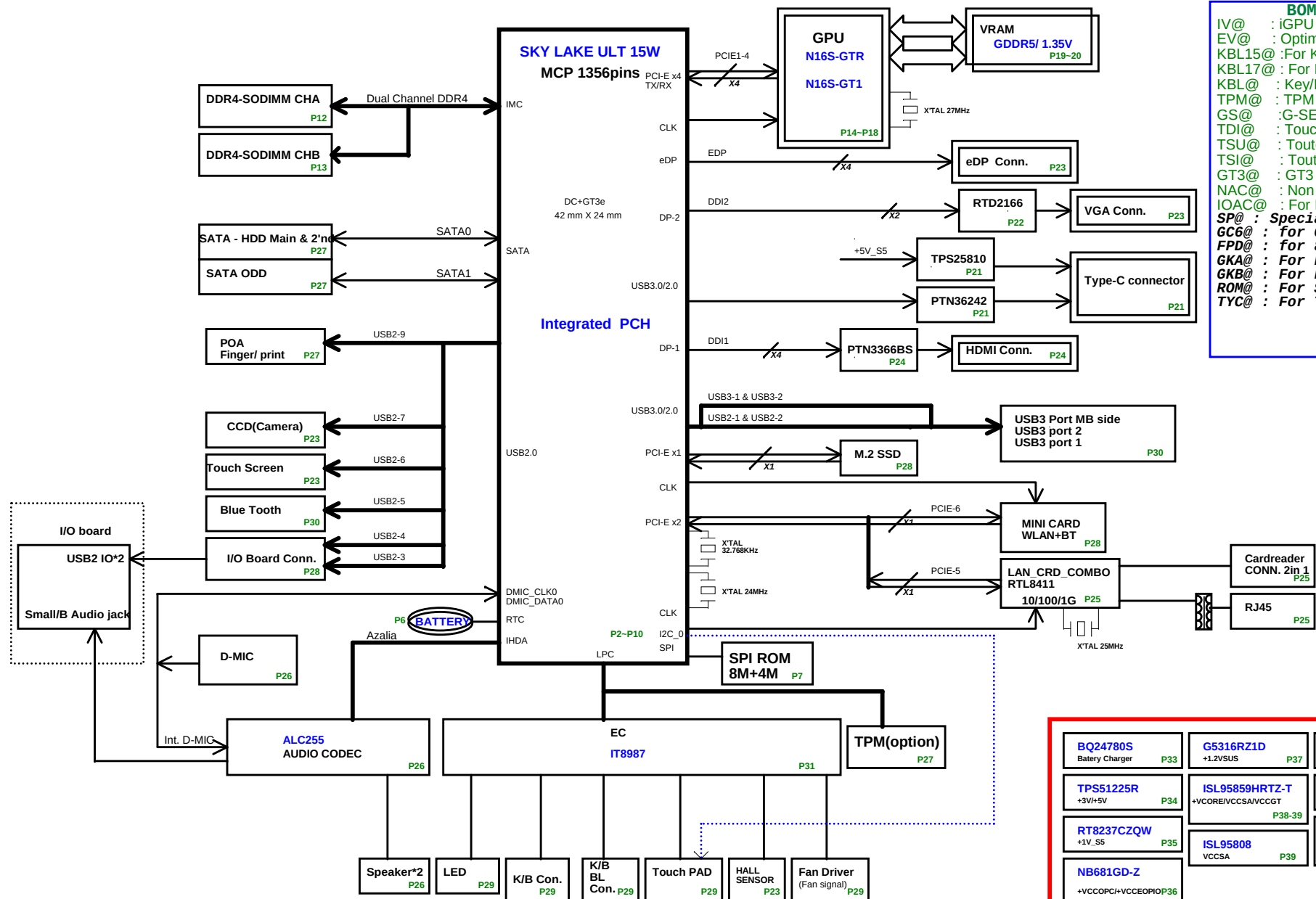


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ZAA Serials SKL ULT SYSTEM BLOCK DIAGRAM



BOM
 IV@ : iGPU
 EV@ : Optimus
 KBL15@ : For Key/B 15"
 KBL17@ : For Key/B 17"
 KBL@ : Key/B backlight
 TPM@ : TPM
 GS@ : G-SENSOR
 TDI@ : Touch PAD I2C
 TSU@ : Touch Screen (USB)
 TSI@ : Touch Screen (I2C)
 GT3@ : GT3 CPU
 NAC@ : Non IOAC
 IOAC@ : For IOAC
SP@ : Special part
 GC6@ : for GC6
 FPD@ : for 8 Pin Finger/P.
 GKA@ : For kill GPU A-chanle.
 GKB@ : For kill GPU B-chanle.
 ROM@ : For SKL or KBL
 TYC@ : For Type-C

BQ24790S Battery Charger P33	G5316RZ1D +1.2VSUS P37	Thermal Protection Discharger P41
TPS51225R +3V/+5V P34	ISL95859HRTZ-T +VCCORE/VCCSA/VCCGT P38-39	UP1658RQKF +VGPU_CORE P42
RT8237CZQW +1V_S5 P35	ISL95808 VCCSA P39	RT8068AZQW +1.05V_GFX/+3V_GFX +1.5V_GFX P43
NB681GD-Z +VCCOPC/+VCCOPROP36		

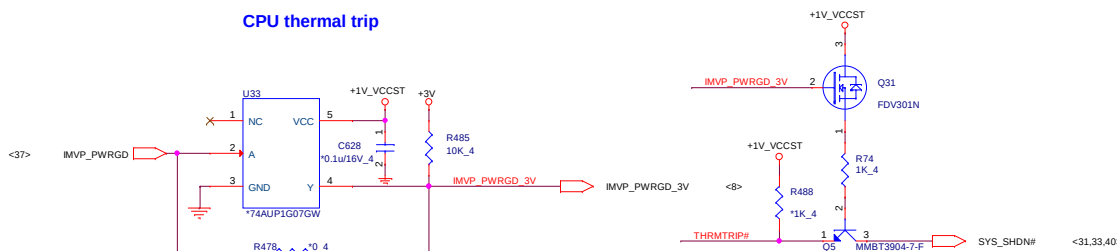
CH6221M9A00
 CH6221M9A01
 CH6221M9A02

CAP CHIP 22U 6.3V(+/-20%, X5R, 0805)H1.25
 CAP CHIP 22U 6.3V(+/-20%, X5R, 0805)H1.25
 CAP CHIP 22U 6.3V(+/-20%, X5R, 0805)H1.25

remove TPM from SKL , KBL keeps it.---- for B2
 add POA FUNCTION, , add 0hm*4 between EC to POA conn & server VST * 7 pcs
 POA (change FP power from 3v to 5v)

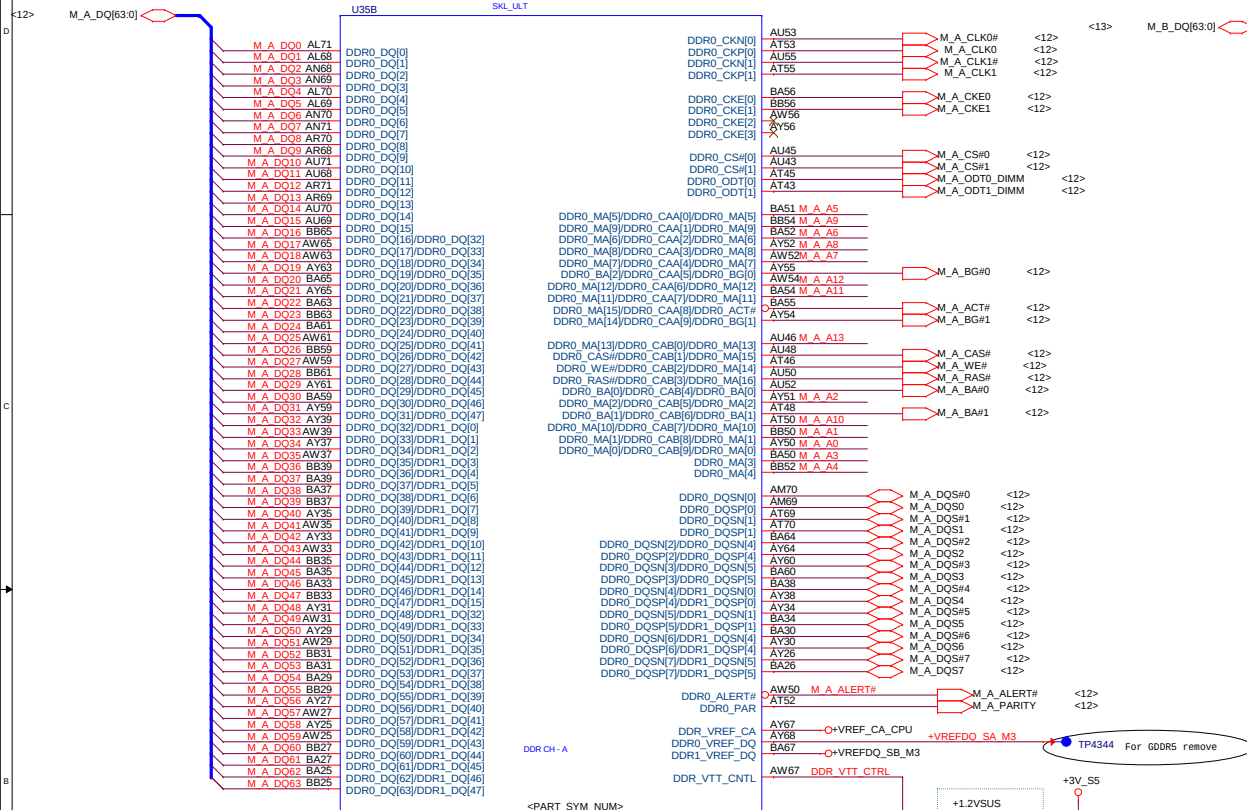
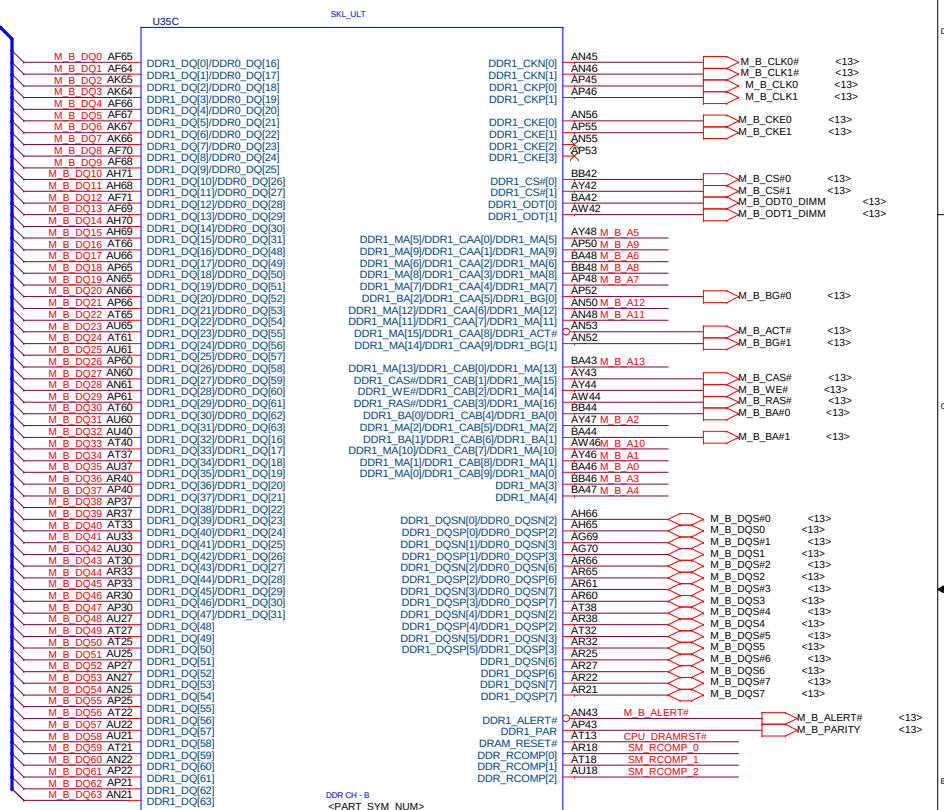
3
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SkyLake ULT (DISPLAY, eDP)



3
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Change Data and DQS to interleave.

SKL ULT (DDR3L)**SKL ULT (DDR3L)**

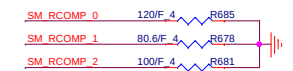
For Sx ,stuff Q? in DDR_VTT_CNTL

DRAM COMP

DRAMRST

CP

DRAM



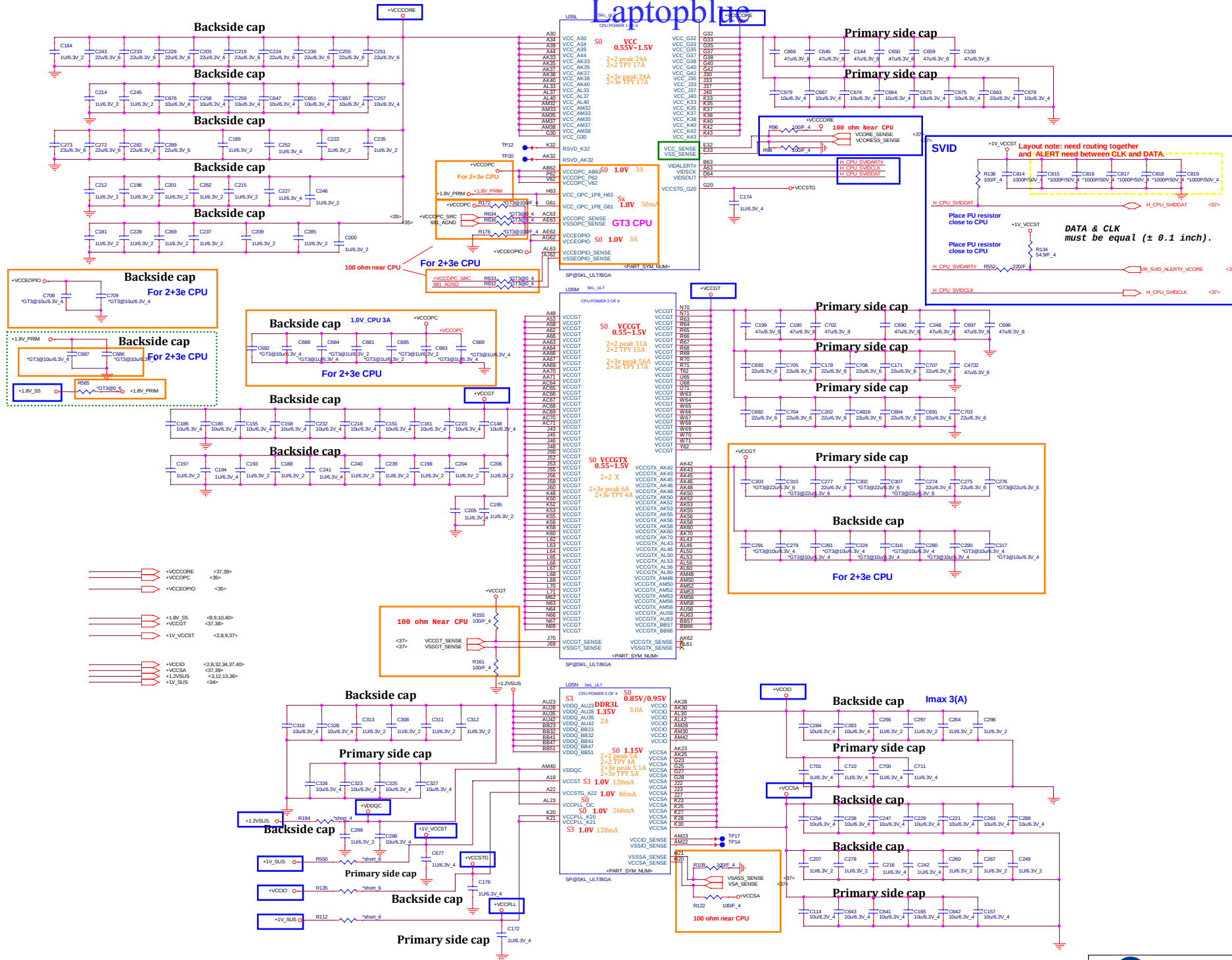
Quanta Computer Inc.

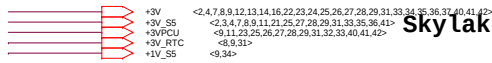


PROJECT : ZAA

Size	Document Number	Rev
	Skylake 2/3 (DDR3 I/F)	1A
Date:	Friday, February 05, 2016	Sheet 3 of 48

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dGPU PEG#4

For Thunderbolt

HDD

ODD

LAN

WIFI

For M.2 SSD -NA

For M.2 SSD -1

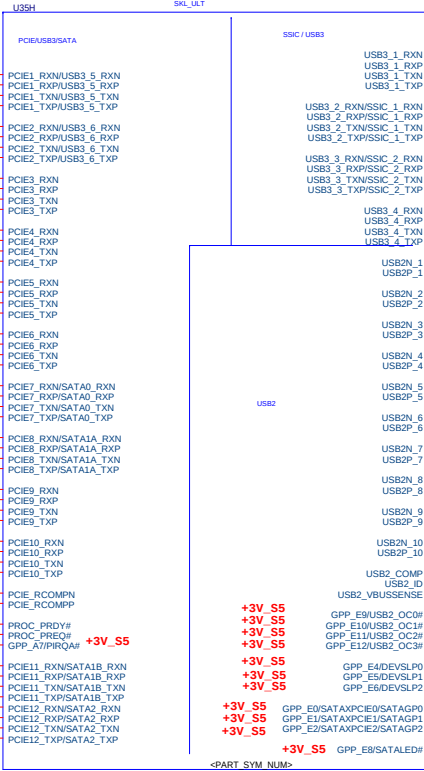
N16S VGA

M.2 SSD

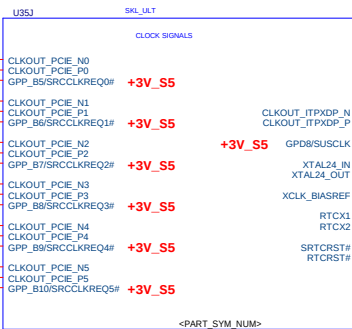
For Thunderbolt

LAN

WLAN

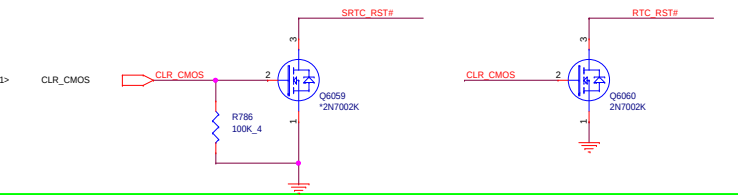


SP@SKL_UL1/BGA

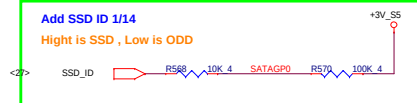
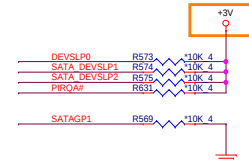
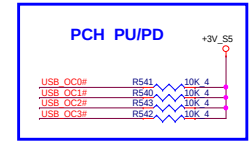


SP@SKL_UL1/BGA

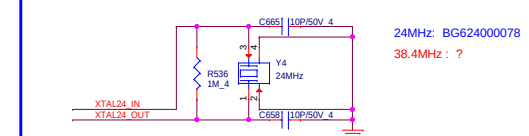
Rev:D add for EC reset RTC



1V power plane
0.71 checklist p14

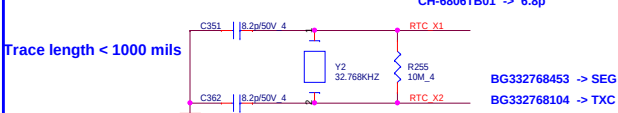


SkyLake-U used 24 MHz (50 Ohm ESR) XTAL

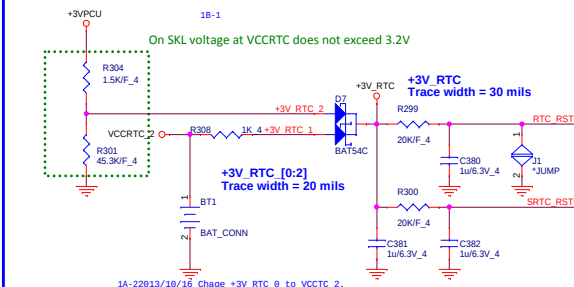


Note: Change Y4 to 38.4 MHz(ESR 30 ohm) for Cannonlake U

RTC Clock 32.768KHz (RTC)

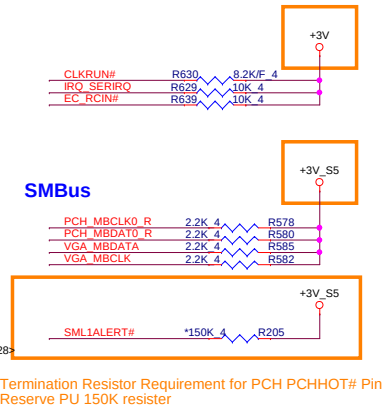
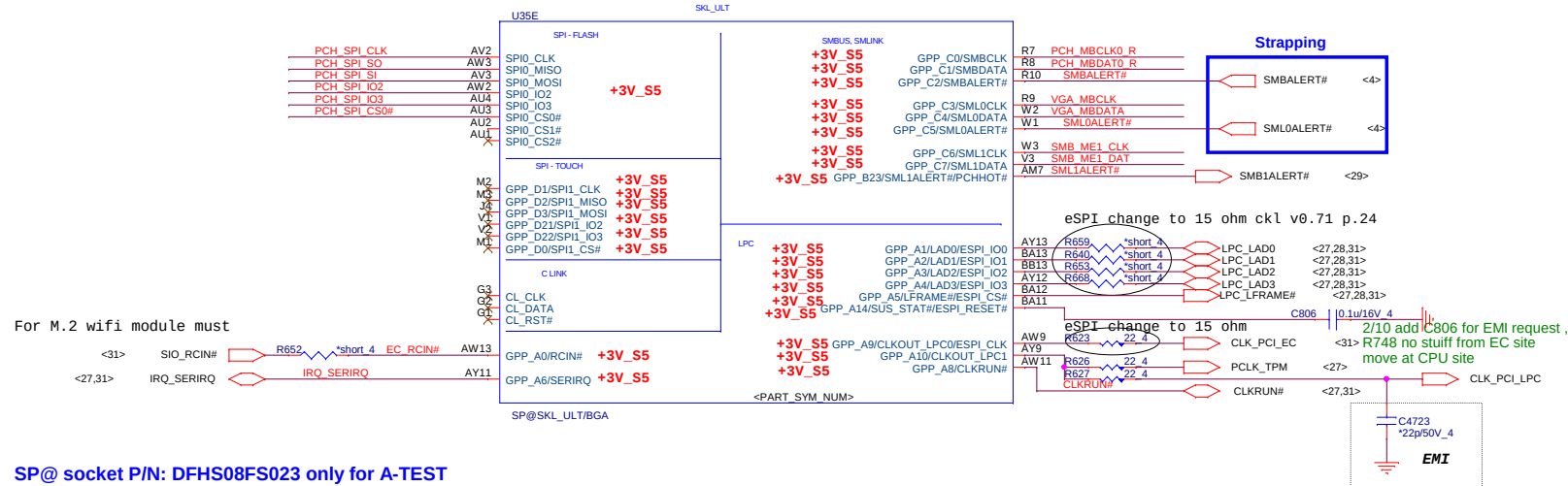


RTC Circuitry (RTC)



- AHL03003057 DBV CR2032
- AHL03003003 VDE CR2032

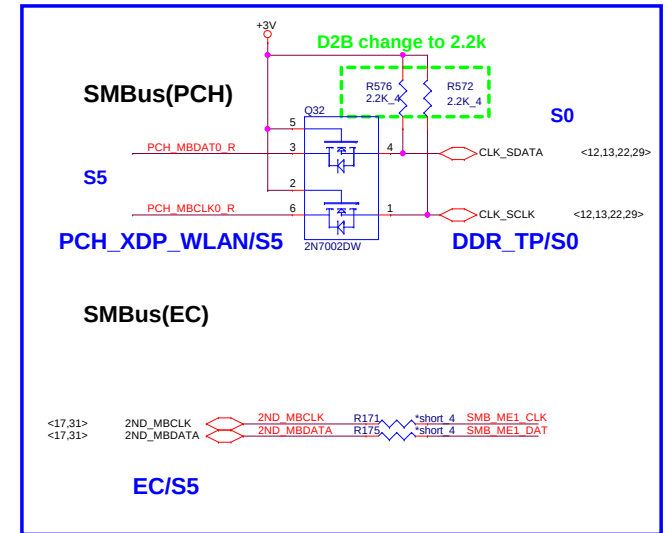
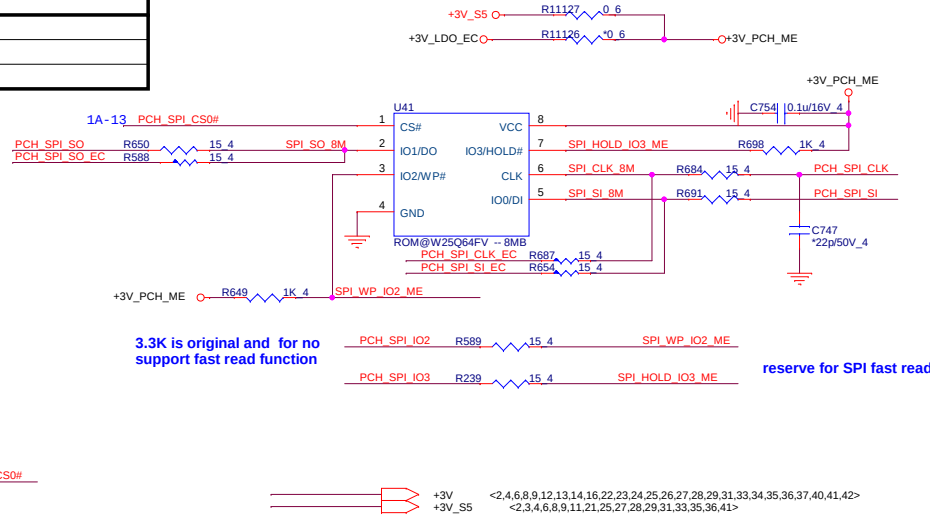
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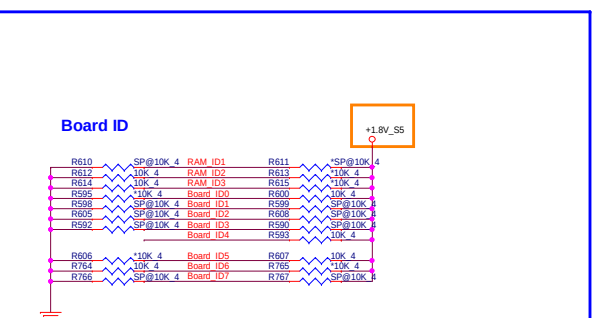
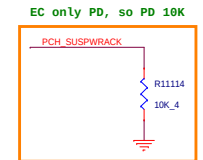
SP@ socket P/N: DFHS08FS023 only for A-TEST

SPI ROM	Vender	Size	Quanta P/N	Vender P/N	Platform
Skylake 3.3V	WND	8M	AKE3EFP0N07	W25Q64FVSSIQ	SKL
	GGD	8M	AKE2EZNOQ00	GD25B64CSIGR	KBL

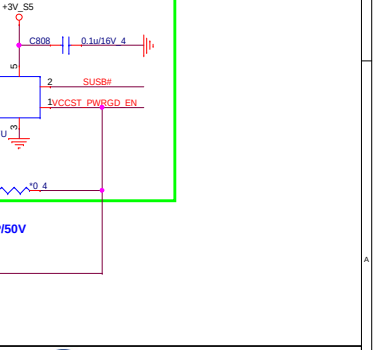
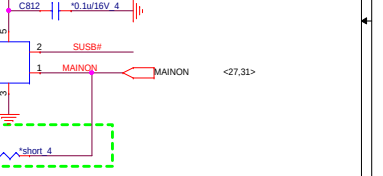
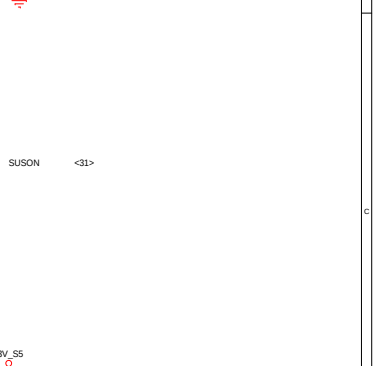
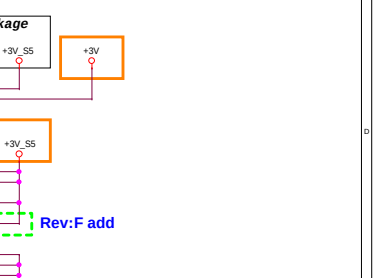
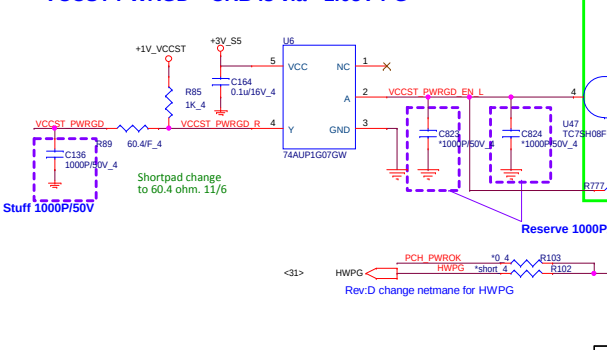
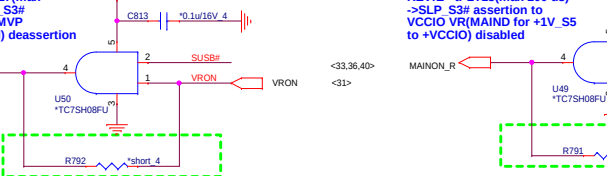
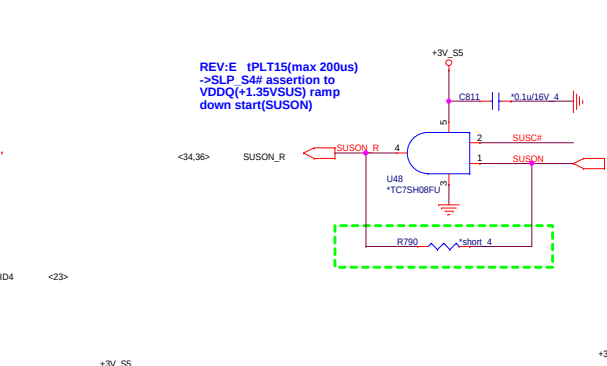
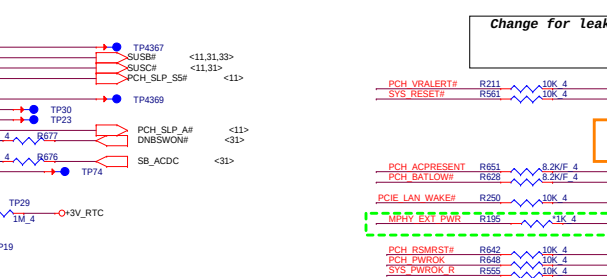
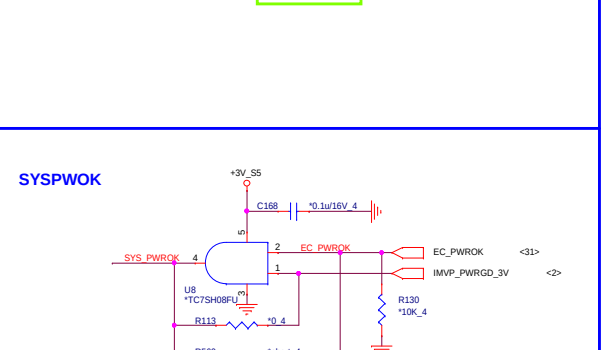
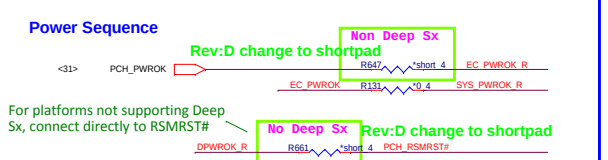
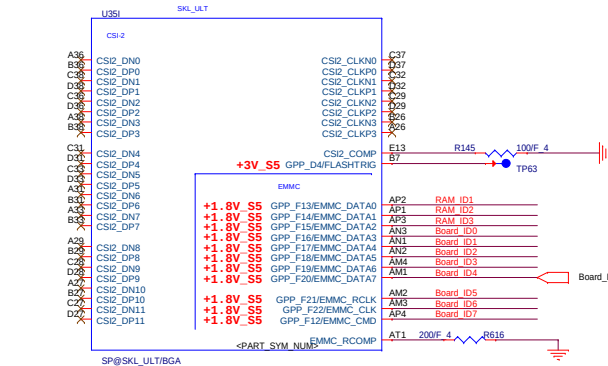
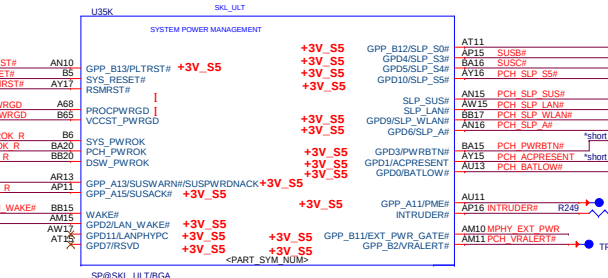
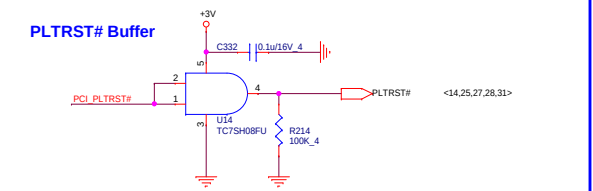
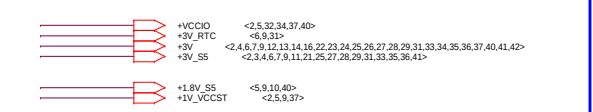
Winbound for SKL / Giga for KBL



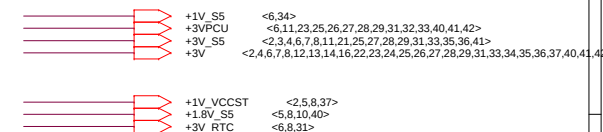
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	Low	High		Low	High
BOARD_ID0	VRAM X32	VRAM X16	BOARD_ID5	14"	15/17"
BOARD_ID1	Non IOAC	IOAC	BOARD_ID6	Reserved (Default)	Reserve
BOARD_ID2	No G-sensor	G-sensor	BOARD_ID7	GPU-> KA (Kill A-channel) (Default)	GPU-> KB (Kill B-channel)
BOARD_ID3	No TPM	TPM			
BOARD_ID4	No touch panel	touch panel			

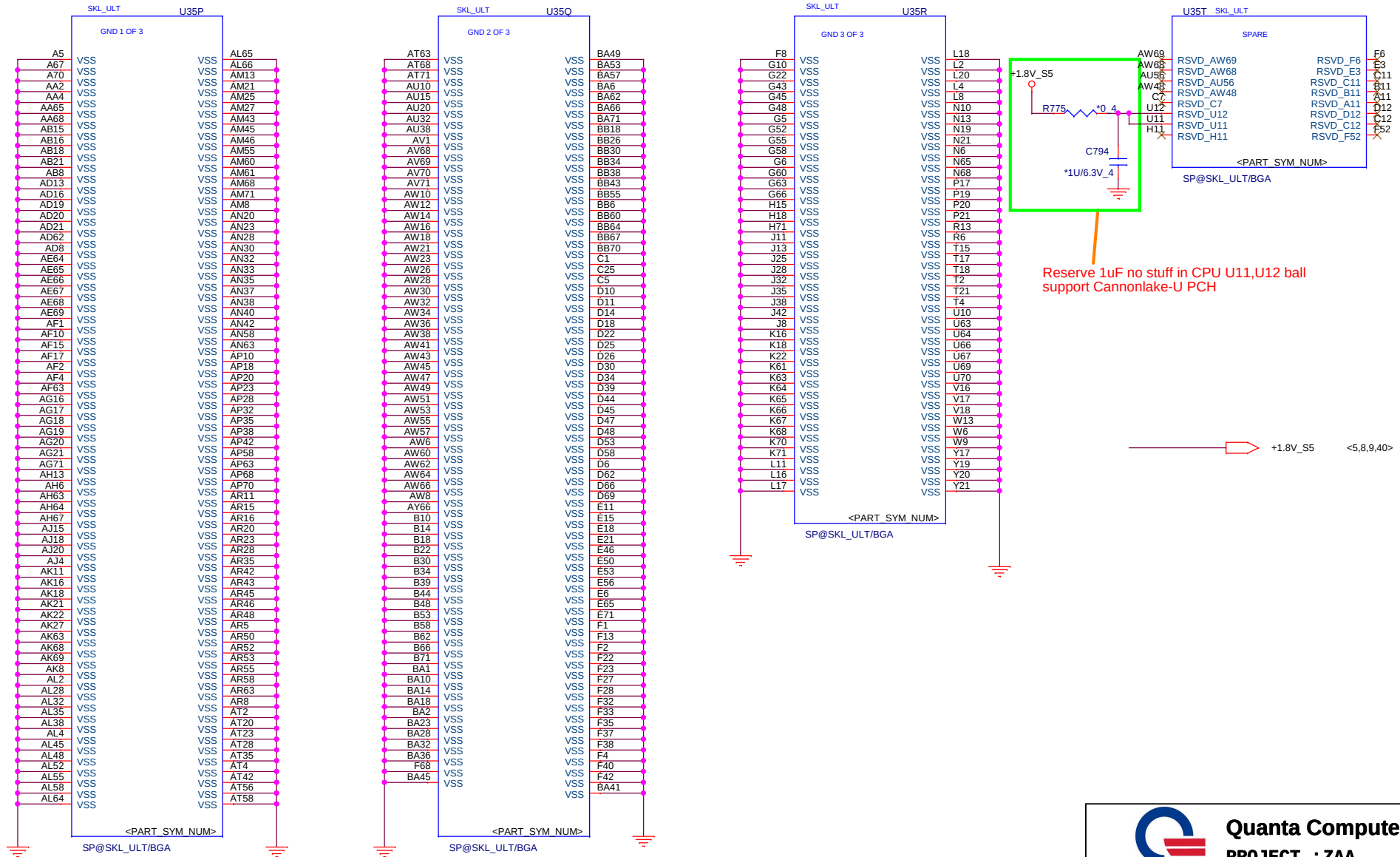


GPIO Group Power Plane



 Quanta Computer Inc. PROJECT : ZAA	
Size	Document Number Skylake PCH-LP 15/19 (POWER)
Date:	Friday, February 05, 2016 Sheet 9 of 48 Rev 1A

Skylake ULT (GND)

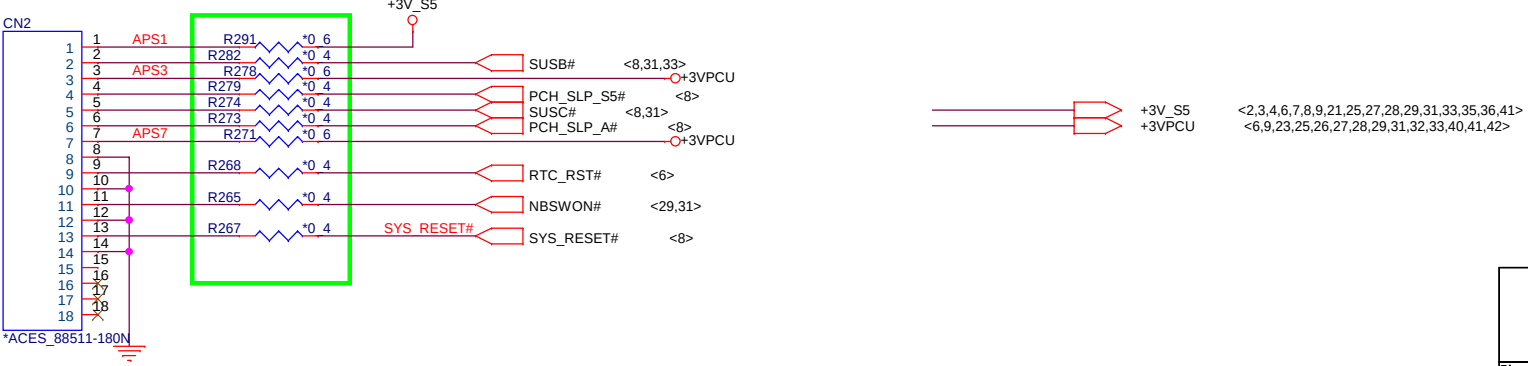


Quanta Computer Inc.
PROJECT : ZAA

Size	Document Number	Rev
	Skylake 10/17/18 (GND)	1A
Date:	Friday, February 05, 2016	Sheet 10 of 48

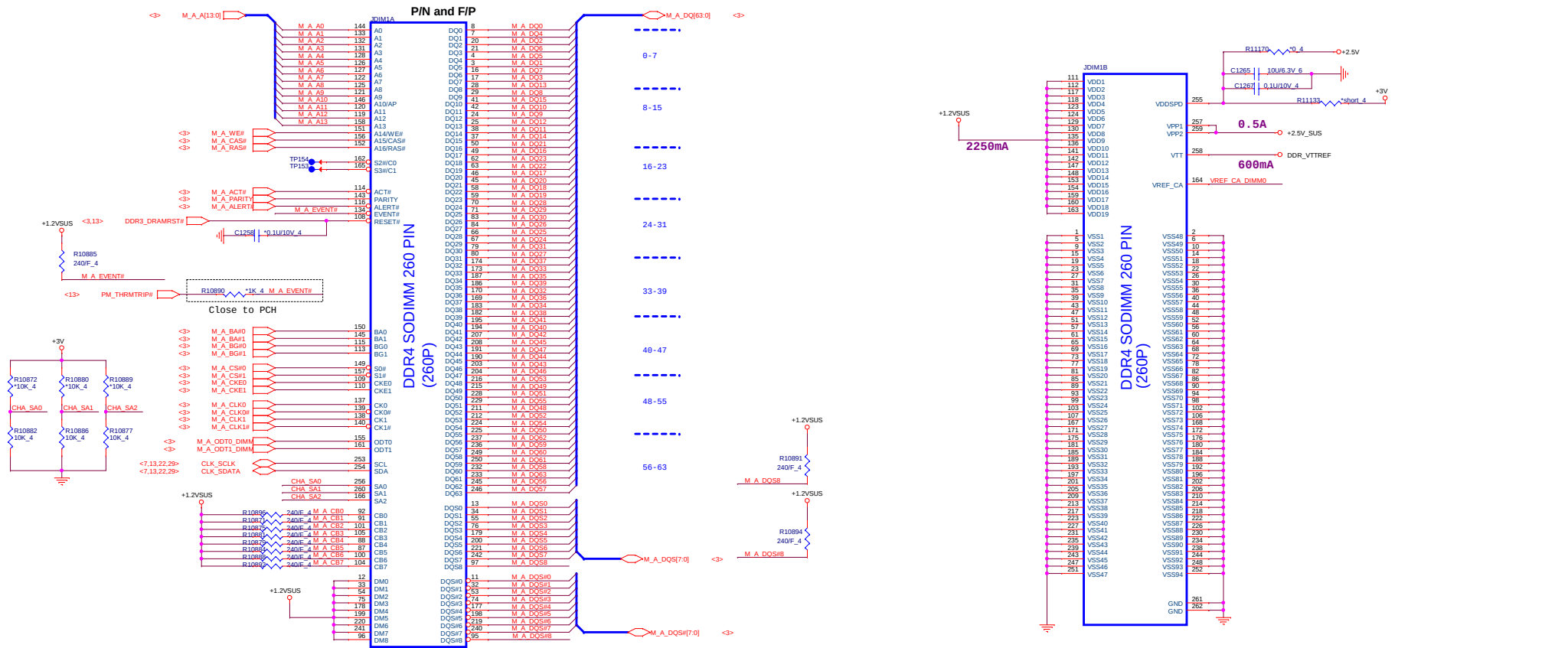


Intel APS Fixture use



3

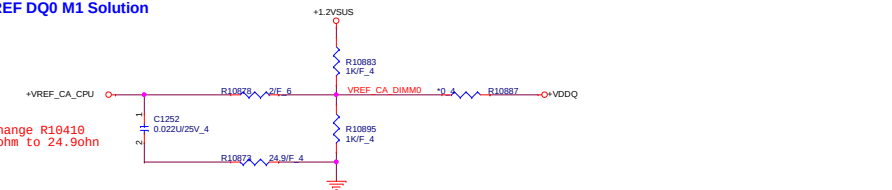
Laptopblue



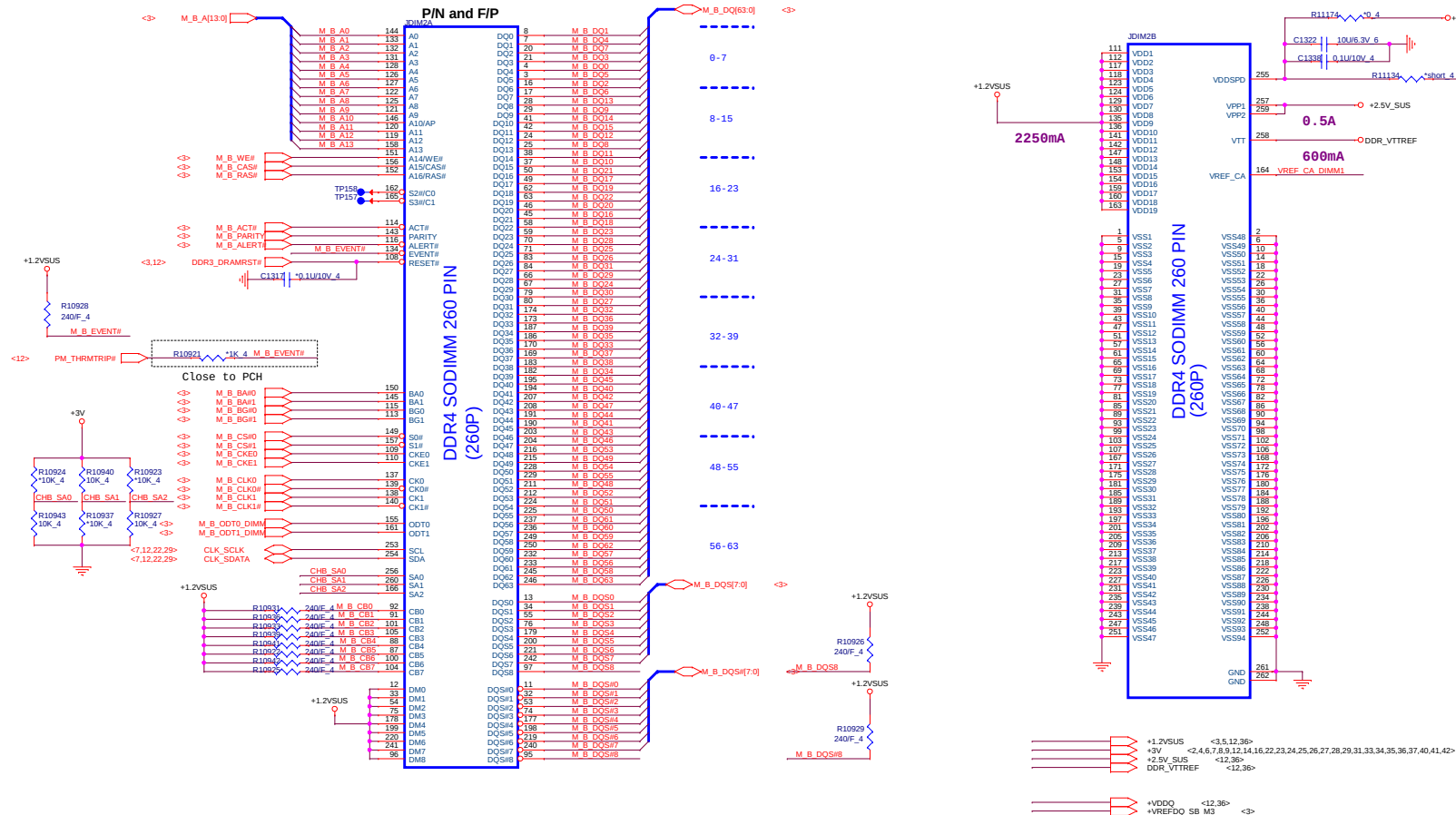
Place these Caps near So-Dimm1.
1uF/10uF 4pcs on each side of connector

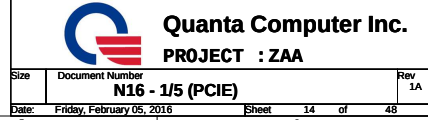


VREF DQ0 M1 Solution

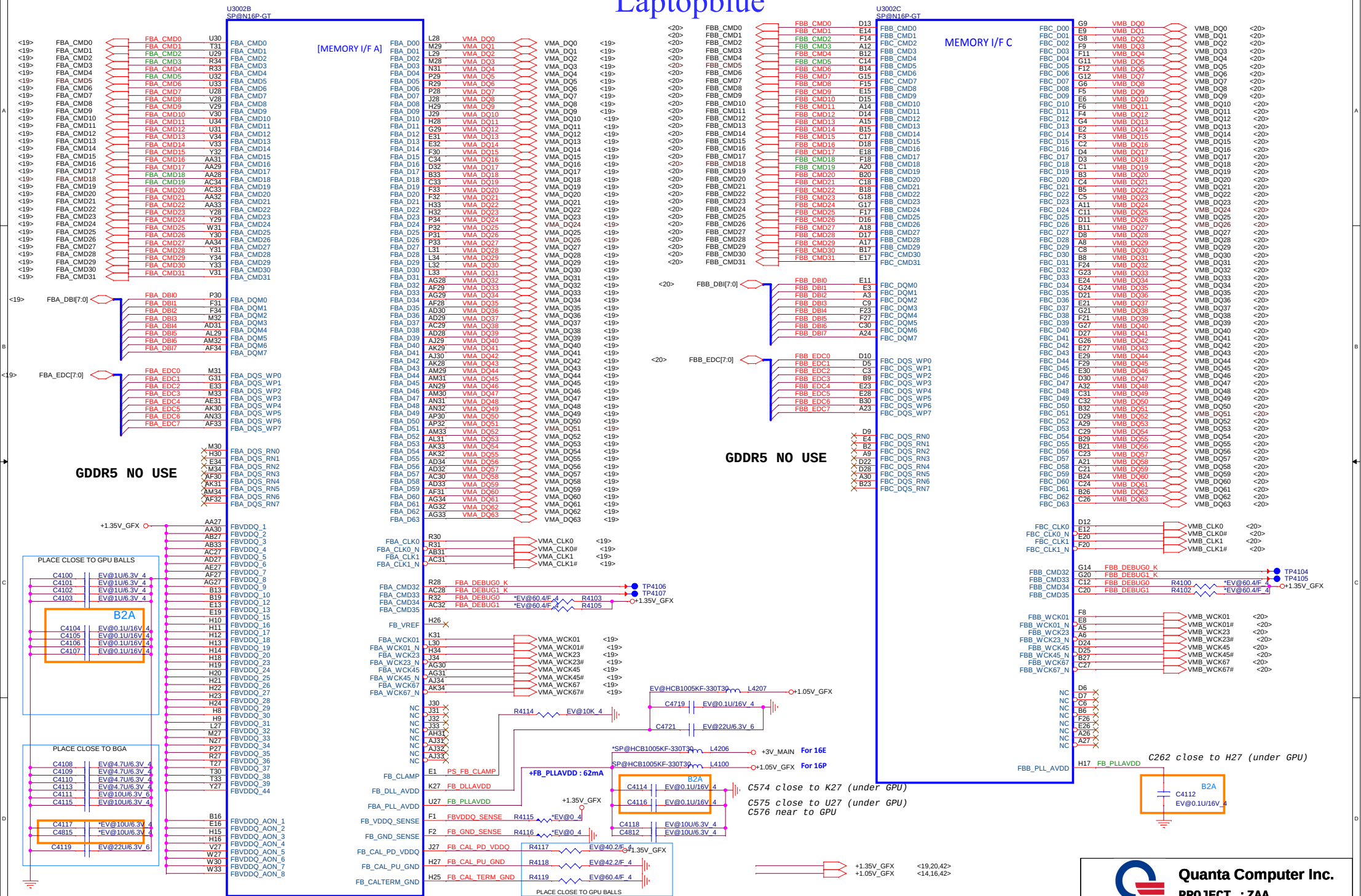


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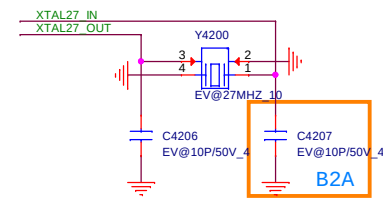
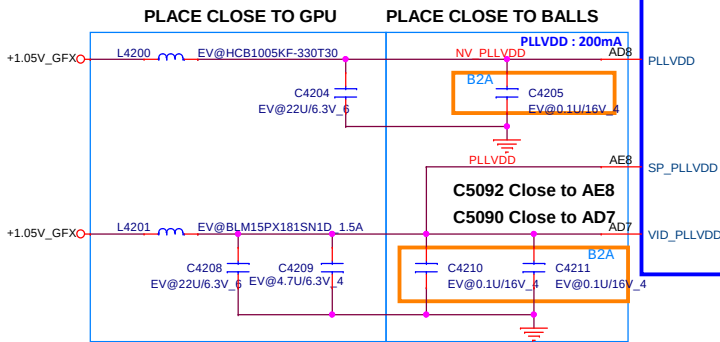
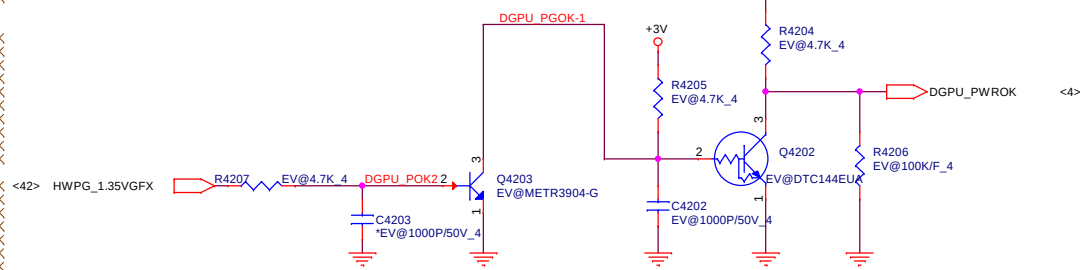
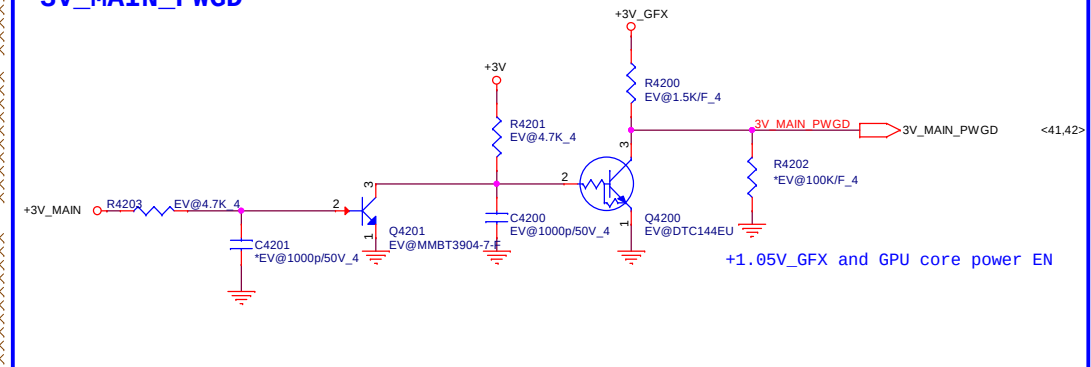


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+3V_MAIN <14,15,17>
 +1.05V_GFX <14,15,42>
 +3V_GFX <14,17,31,42>
 +3V <2,4,6,7,8,9,12,13,14,22,23,24,25,26,27,28,29,31,33,34,35,36,37,40,41,42>



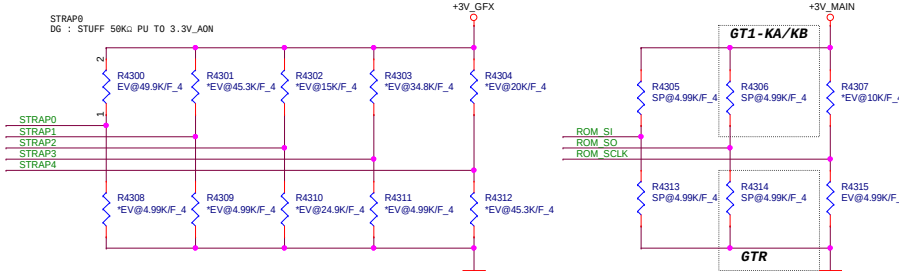
3V_MAIN_PWGD



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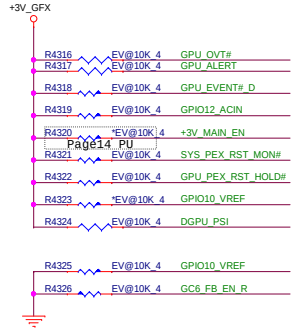
Default setting :

x16 (8L)					
#2					
SKU15 (B6)	SKU16 (B6)	SKU17 (B5)	SKU19 (B5)	SKU18	SKU20
GT3	(B6)			For VRAM Timing Tuning	
I-6200U	I7-6500U	I-6200U	I-6200U	I-6200U	I-6200U
N16S-GTR	N16S-GTR	940M KA	940M KB	940M KA	940M KB
4G	4G	4G	4G	4G	4G
512x16x4	512x16x4	512x16x4	512x16x4	512x16x4	512x16x4
K4G80325FB-HC03 (Samsung)	MT51J256M32H-F 60 A(Micron)	K4G80325FB-HC03 (Samsung)	K4G80325FB-HC03 (Samsung)	MT51J256M32H-F 60 A(Micron)	MT51J256M32H-F 60 A(Micron)



(default)		
N16S-GTR	GB4b-128	0x134D
N16S-GT1-KA	GB4b-128	0x179c
N16S-GT1-KB	GB4b-128	0x179c

Resistor P/N
 4.99K ---> CS24992FB26
 10K ---> CS31002FB26
 15K ---> CS31502FB24
 20K ---> CS32002FB29
 24.9K ---> CS32492FB16
 30.1K ---> CS33012FB18
 34.8K ---> CS33482FB22
 45.3K ---> CS34532FB18
 49.9K ---> CS34992FB10



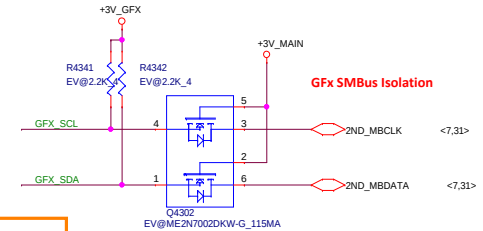
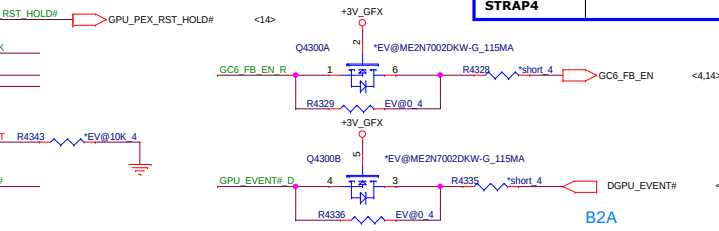
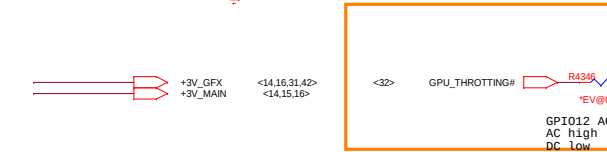
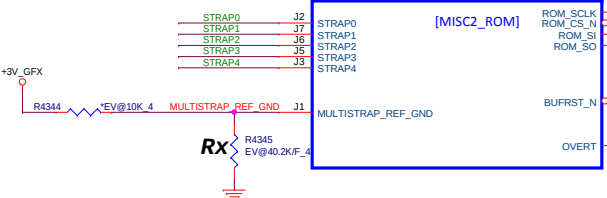
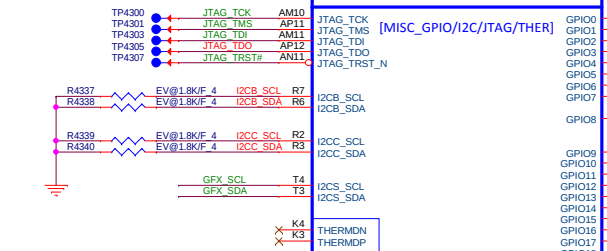
Reserve PU/PD for Debug



	PU +3V_MAIN	PD
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

Mutil-level mode strapping:

- 1.ROM_SCLC = 4.99K PD
 2.ROM_SO = 4.99K PD for GTR ;
 4.99K UP for GT1-KA/KB
 3.ROM_SI= VRAM Configuration Table
 4.STRAP0 = 49.9k PU
 5.Strap4~1 = Reserve Pull up and Pull down



N16S-GTR VRAM Configuration Table: *N16S-GTR-B-A2 GM108-770-A2 AJ0N16S0T24*

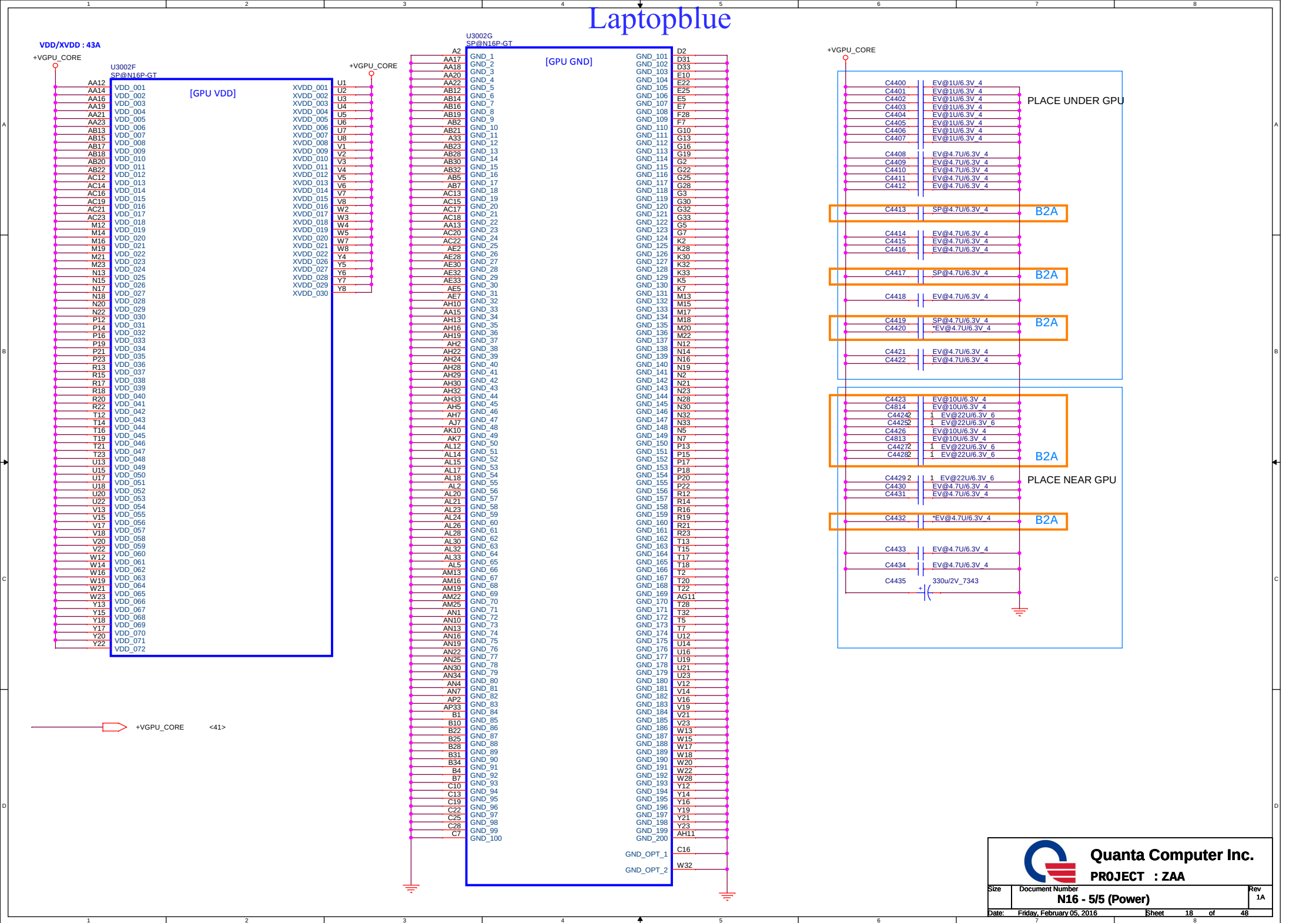
	ROM_SI	DESCRIPTION	Vendor	Vendor P/N	STN P/N	ROM_SI
4GbX2 (1GB)	0011 (0x3) 0110 (0x6)	GD0RS 128MBX32.2500MHZ	SAMSUNG HYNIX	K4641325FC-HC03 --C d1e H56C4H24AJR-TZC --A d1e	AKG56PD7505 AKG56PWUT21	20K Pull down 34.8K Pull down
4GbX4 (2GB)	0011 (0x3) 0110 (0x6)	GD0RS 256MBX16.2500MHZ	SAMSUNG HYNIX	K4641325FC-HC03 --C d1e H56C4H24AJR-TZC --A d1e	AKG56PD7505 AKG56PWUT21	20K Pull down 34.8K Pull down
8GbX2 (2GB)	0000 (0x0) 0001 (0x1)	GD0RS 256MBX32.2500MHZ	SAMSUNG MICRON	K46800325FB-HC03 --B d1e MT51J256B32HF-60:A--A d1e	AKG506D7502 AKG56LUTL04	4.99K Pull down 10K Pull down
8GbX4 (4GB)	0000 (0x0) 0001 (0x1)	GD0RS 512MBX16.2500MHZ GD0RS 512MBX16.2500MHZ	SAMSUNG MICRON	K46800325FB-HC03 --B d1e MT51J256B32HF-60:A--A d1e	AKG506D7502 AKG56LUTL04	4.99K Pull down 10K Pull down

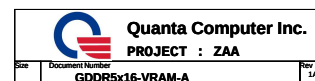
N16S-GT1-KA/KB-A2 VRAM Configuration Table:

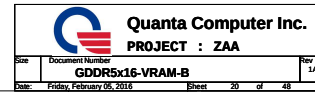
	ROM_SI	DESCRIPTION	Vendor	Vendor P/N	STN P/N	ROM_SI
4GbX2 (1GB)	0011 (0x3) 0110 (0x6)	GD5R 128MBX32.2500MHZ GD5R 128MBX32.2500MHZ	SAMSUNG HYNIX	K4G41325FC-HC03 -- -A die H5G64H24AJR-TZC	AKG5P6WT505 AKG5P6WTW21	20K Pull down 34.8K Pull down
4GbX4 (2GB)	0011 (0x3) 0110 (0x6)	GD5R 256MBX16.2500MHZ GD5R 256MBX16.2500MHZ	SAMSUNG HYNIX	K4G41325FC-HC03 -- -A die H5G64H24AJR-TZC	AKG5P6WT505 AKG5P6WTW21	20K Pull down 34.8K Pull down
8GbX2 (2GB)	0000 (0x8) 0001 (0x9)	GD5R 256MBX32.2500MHZ GD5R 256MBX32.2500MHZ	SAMSUNG MICRON	K4G680325FB-HC03 -- -B die MT513256M32HF-60: -A die	AKG5O6WT502 AKG5L6UTL04	4.9K Pull up 10K Pull up
8GbX4 (4GB)	0000 (0x8) 0001 (0x9)	GD5R 512MBX16.2500MHZ GD5R 512MBX16.2500MHZ	SAMSUNG MICRON	K4G680325FB-HC03 -- -B die MT513256M32HF-60: A -A die	AKG5O6WT502 AKG5L6UTL04	4.9K Pull up 10K Pull up

(GB4b-128)					
	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0000
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	Refer table
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE	0000 ---GTR 1000 ---GT1/KA/KB [Stuff 49.9K PU]
STRAP0	Keep footprint to PU to 3V3_AON and PD to GND				[Do Not Stuff]
STRAP1	Keep footprint to PU to 3V3_AON and PD to GND				
STRAP2					
STRAP3					
STRAP4					

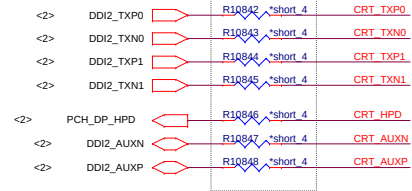
Laptopblue



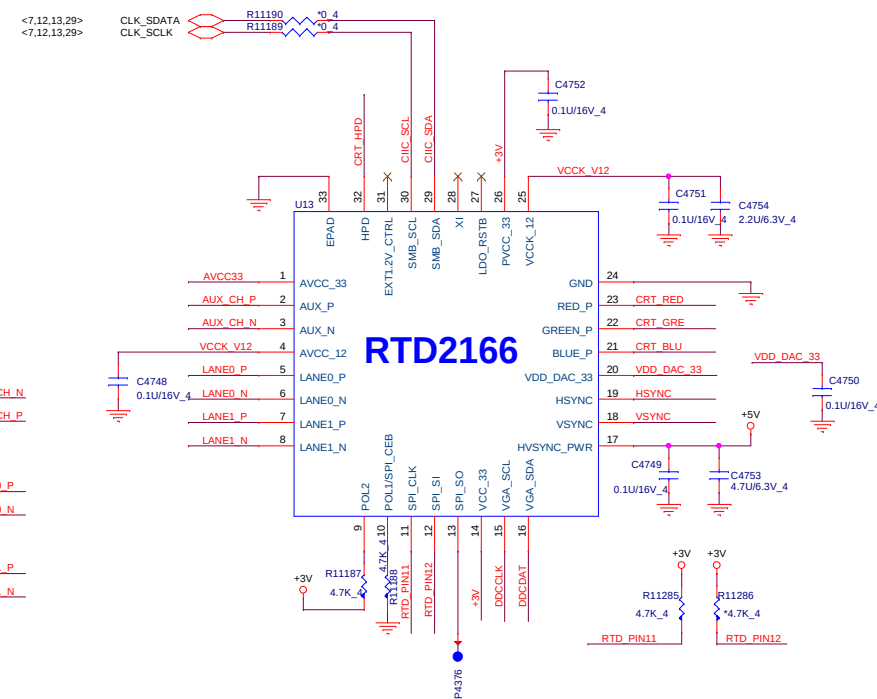
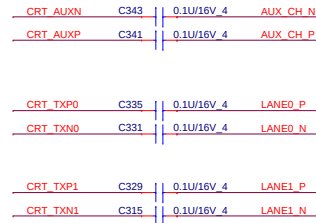
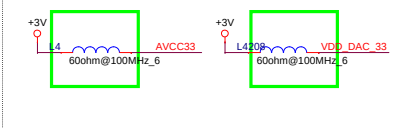




Close to CPU side of CAP.



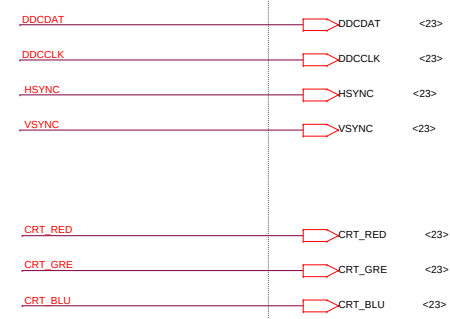
Power



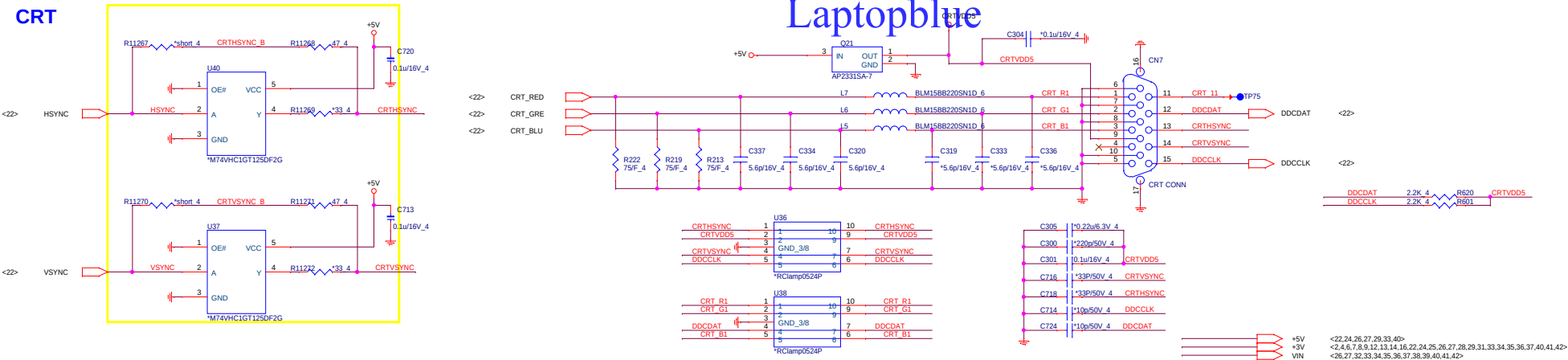
- Note:
- 1- C1,C3,C4,C5,C11,C16, C21 should be placed close to chip
 - 2- C5 should be X5R material
 - 3- R6, R7, R8 should be 75 ohm with +/-1%
 - 4- Suggest to connect Pin 29 and Pin 30 to PCH SMBUS for debug purpose.
 - 5- This configuration is for internal ROM mode and using embedded LDO mode.



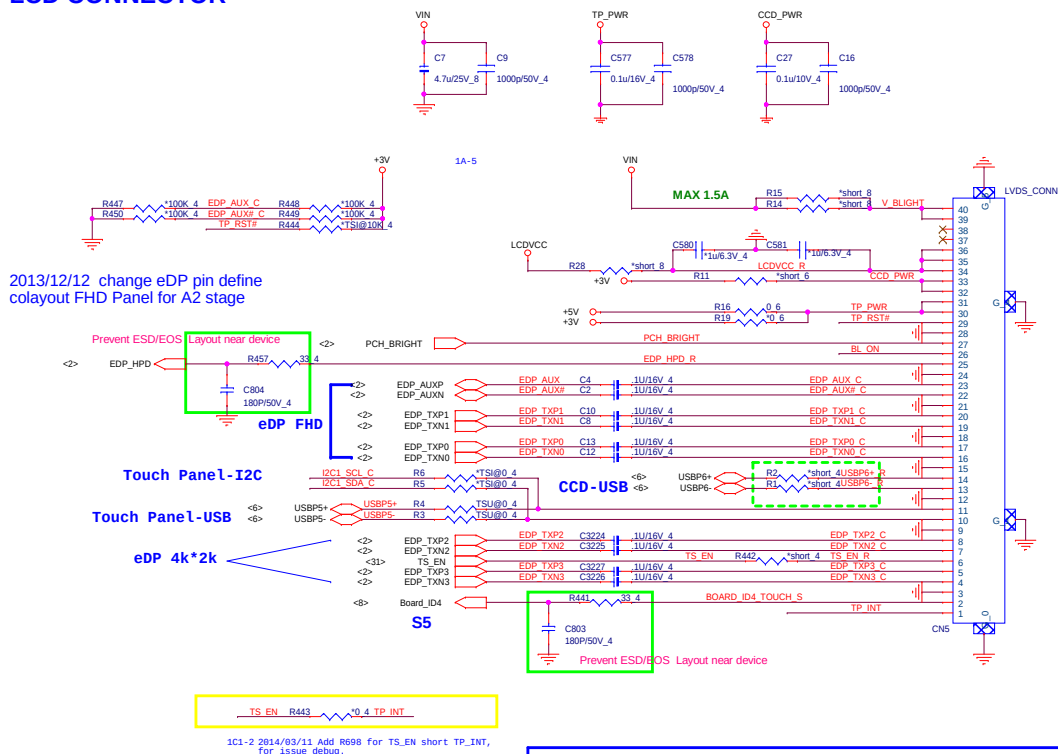
VGA



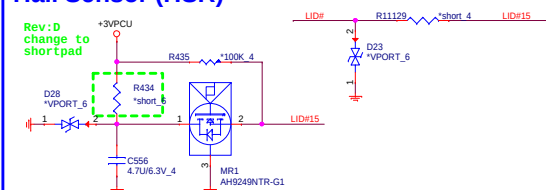
CRT



LCD CONNECTOR

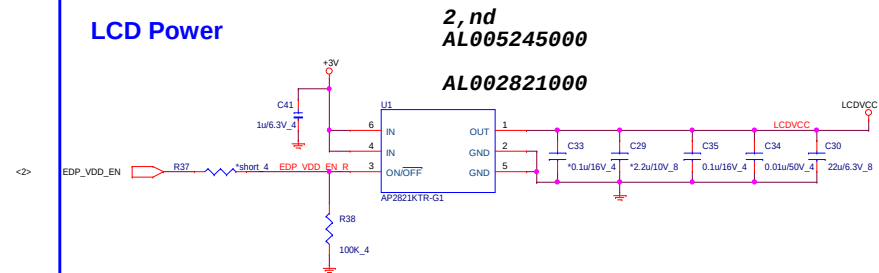


Hall Sensor (HSR)

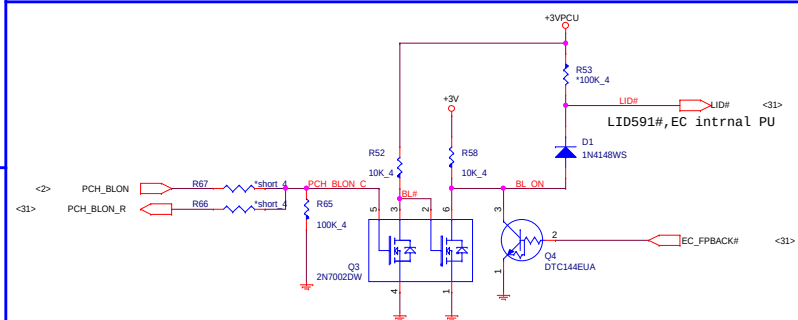
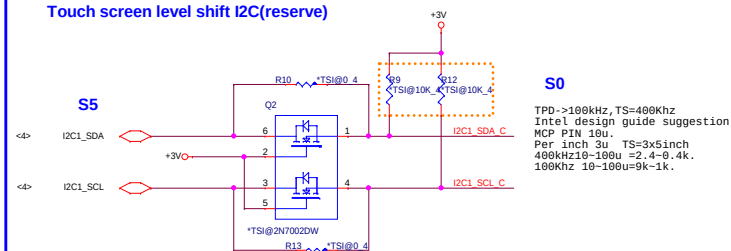


AL009132001 (default)
AL008132004
AL008251000

LCD Power



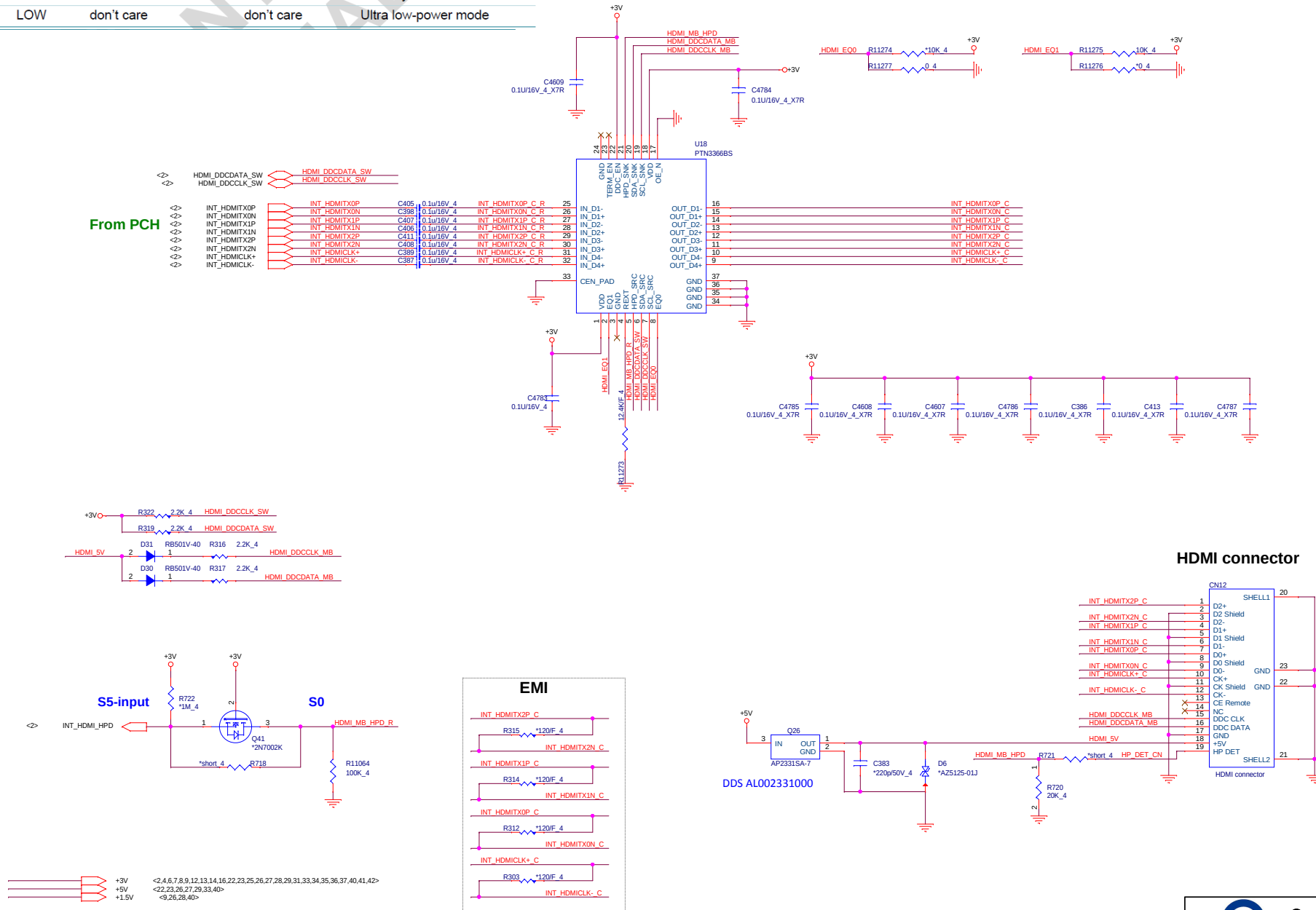
Touch screen level shift I2C(reserve)

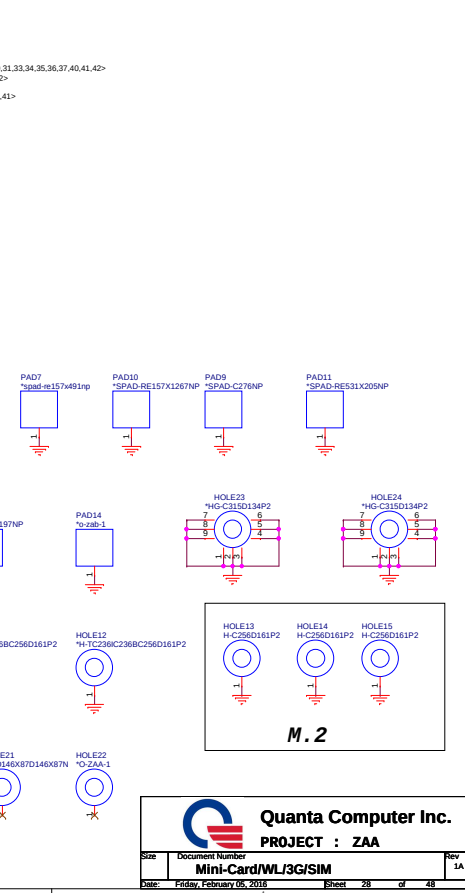
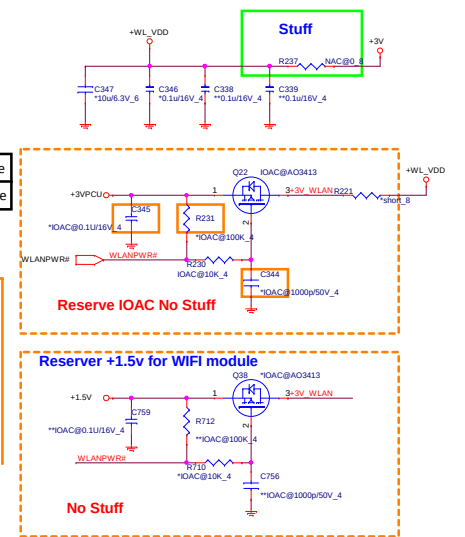


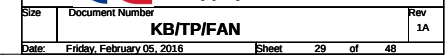
1B-3 2013/12/10 change Q3.3 from +3V to +3VPCU.

3
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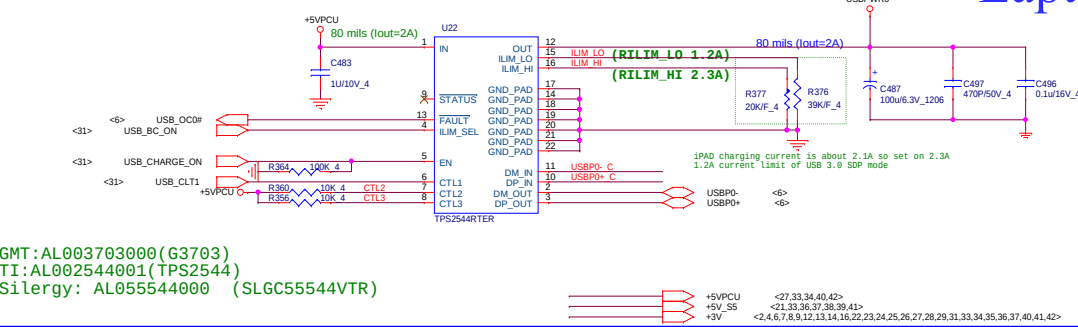
OE_N	DDC_EN	HPD_SINK	Source output	PTN3366 power mode
LOW	HIGH	HIGH	source active	Active mode; DDC active
LOW	LOW	LOW	don't care	Standby mode
HIGH	LOW	don't care	don't care	Ultra low-power mode





[illegible][illegible][illegible][illegible][illegible]

USB Charger to 3.0 (UBC)



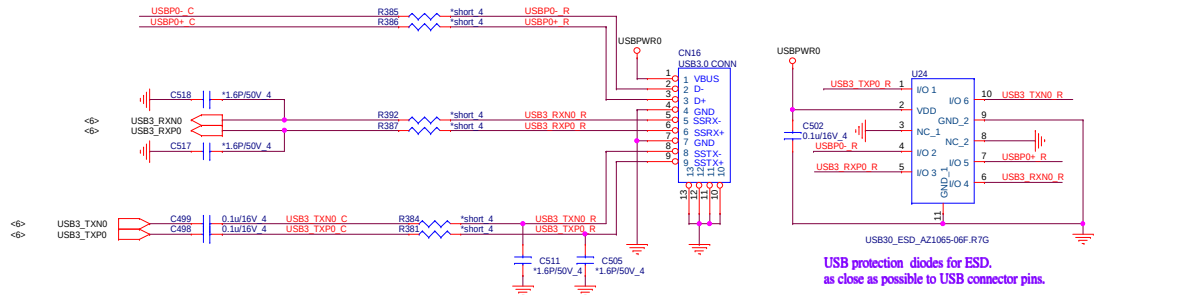
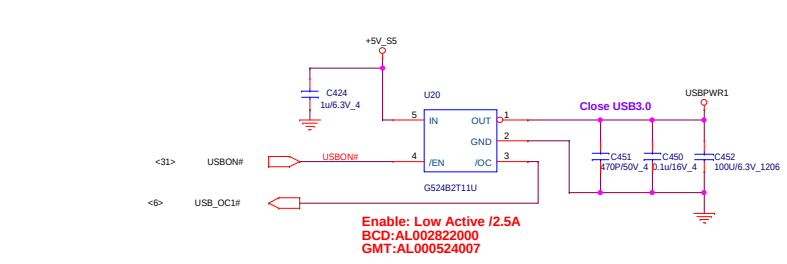
GMT:AL003703000(G3703)
TI:AL002544001(TPS2544)
Silergy: AL055544000 (SLGC55544VTR)

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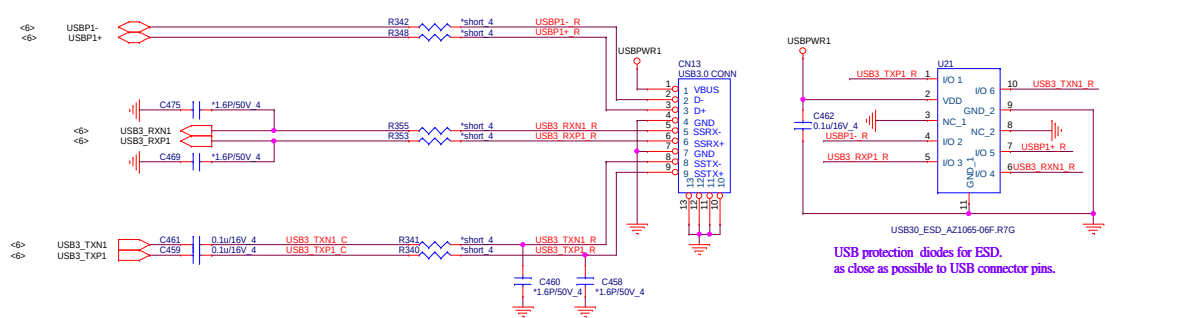
	CTL1	CTL2	CTL3	ILIM_SEL
SDP	1	1	1	0
CDP	1	1	1	1
DCP	0	1	1	X

RILIM_LO is optional and the ILIM_LO pin may be left unconnected if the following conditions are met:
1. ILIM_SEL is always set high
2. Load Detection - Port Power Management is not used
3. Mouse / keyboard wake function is not used
If conditions 1 and 2 are met but the mouse / keyboard wake function is also desired, it is recommended to use RILIM_LO < 80.6 kΩ.
The following equation programs the typical current limit:
(1) $I_{OS\_typ}(mA) = 50,250 / (RILIM\_XX(K\Omega) + 0.1)$
RILIM_XX corresponds to either RILIM_HI or RILIM_LO as appropriate.

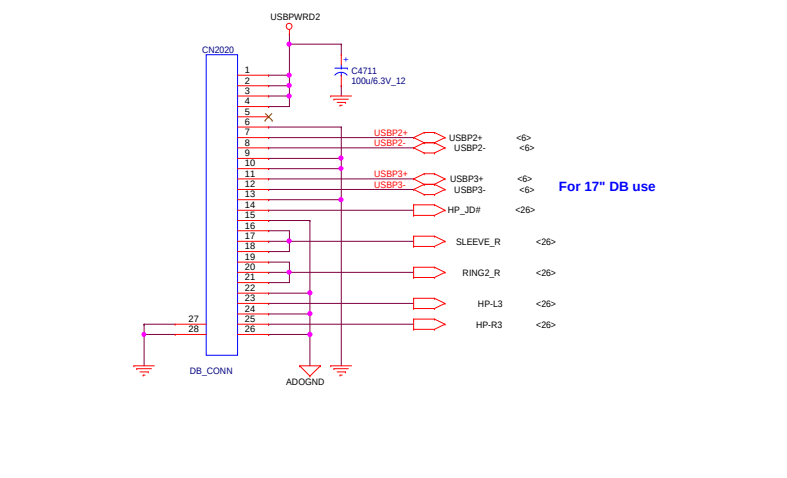
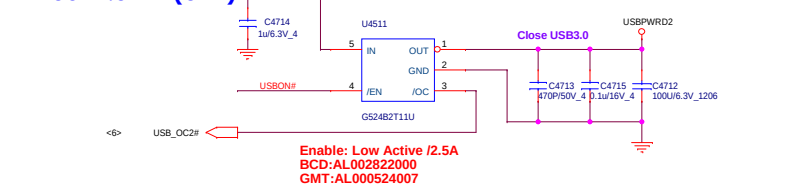
USB 3.0 Connector (UB3)

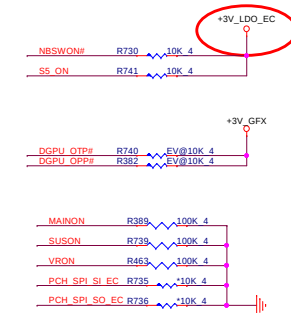
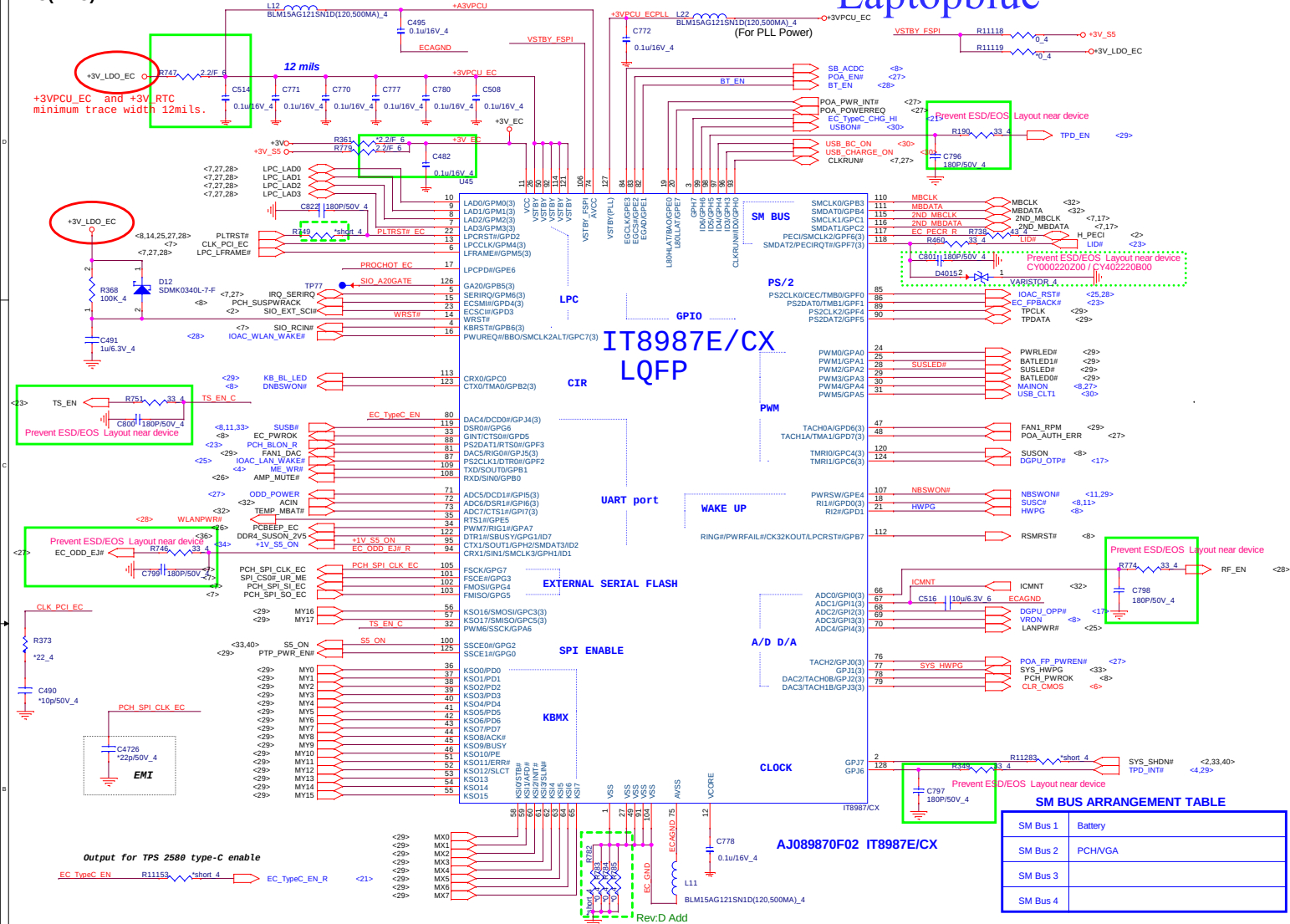


USB3.0 conn, 2'nd : DFHS09FR679

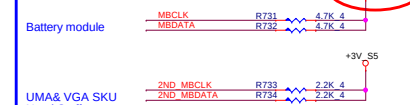


USB2.0 DB (UB2)



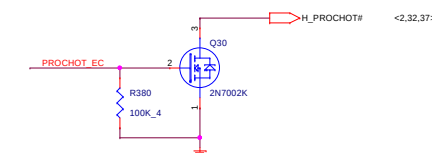


SM BUS PU(KBC)



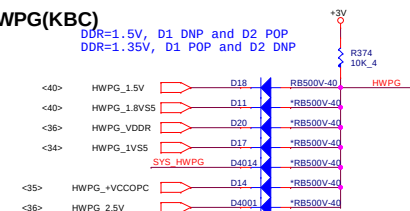
Battery module

UMA& VGA SKU
Need Stuff



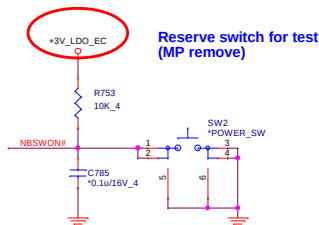
HWPG(KBC)

DDR=1.5V, D1 DNP and D2 POP
DDR=1.35V, D1 POP and D2 DNP

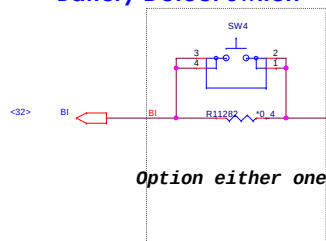


SM Bus 1	Battery
SM Bus 2	PCH/VGA
SM Bus 3	
SM Bus 4	

Battery Detect Switch

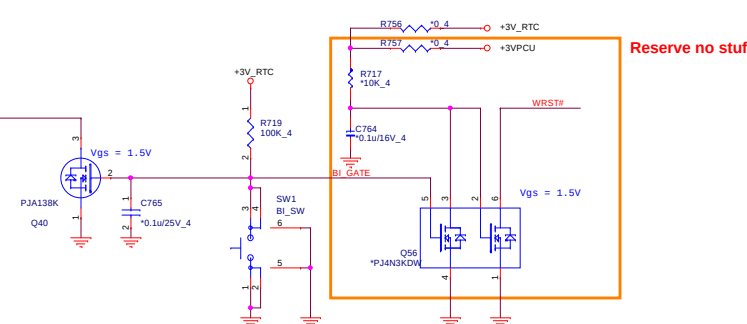


Reserve switch for test
(MP remove)

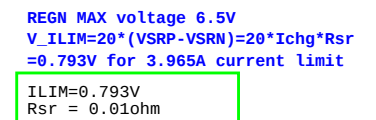


Option either one

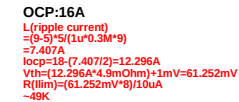
Reset SW (FSW)



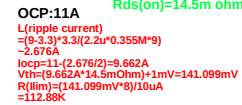
- Reserve no stuff



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Power auto recovery


$$I_2 = 9.662 \text{ A}$$


TDC : 3.6A
PEAK : 4.8A
Width : 160mil

TDC : 1.65A
PEAK : 2.2A
Width : 80mil

TDC : 3.15A
PEAK : 4.2A
Width : 140mi

TDC : 3A
PEAK : 4A
Width : 120mil

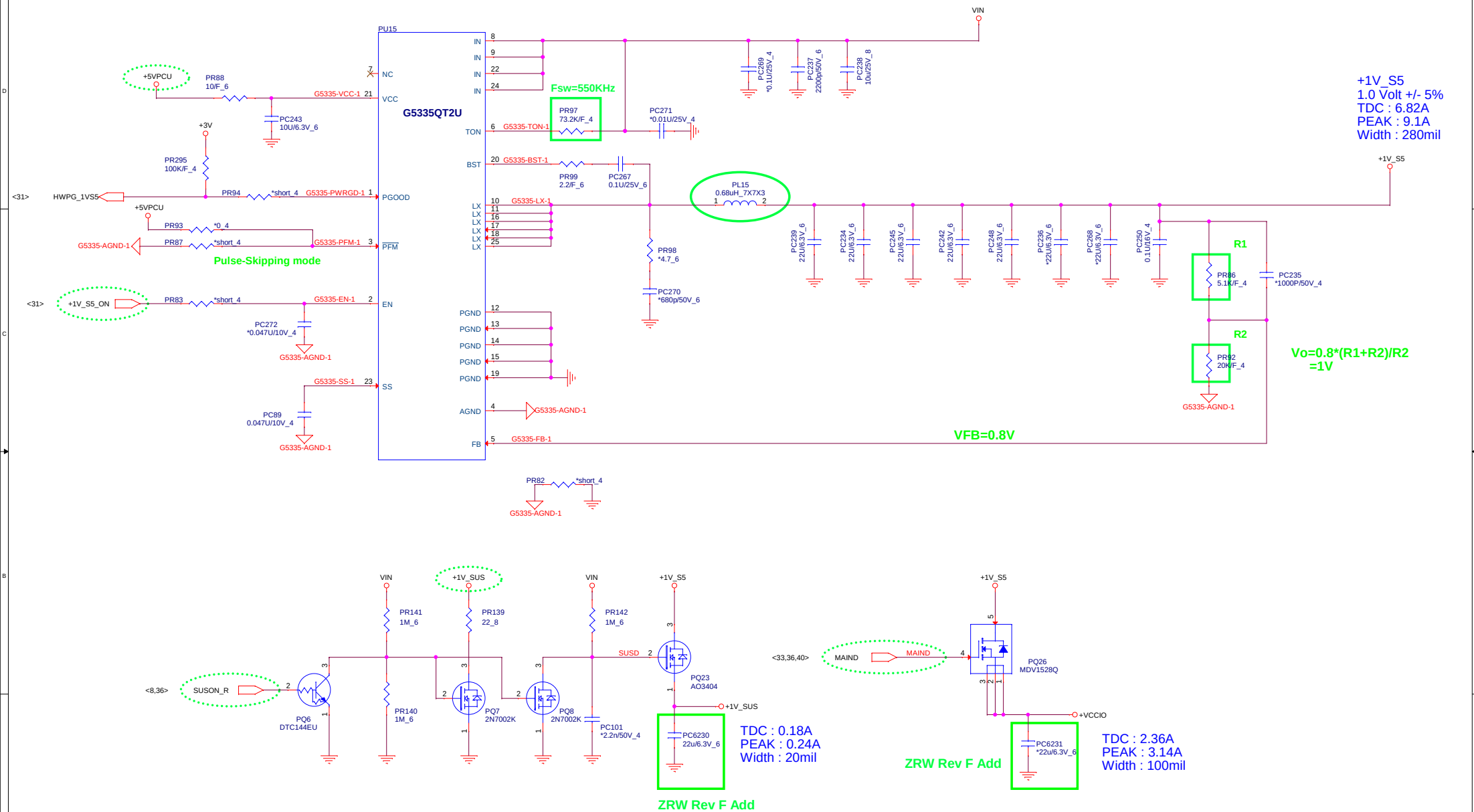
Soft-Start



B2A
S0->S5 & S0->S3
Power off sequence under 200us
SUSB# -> VCCIO

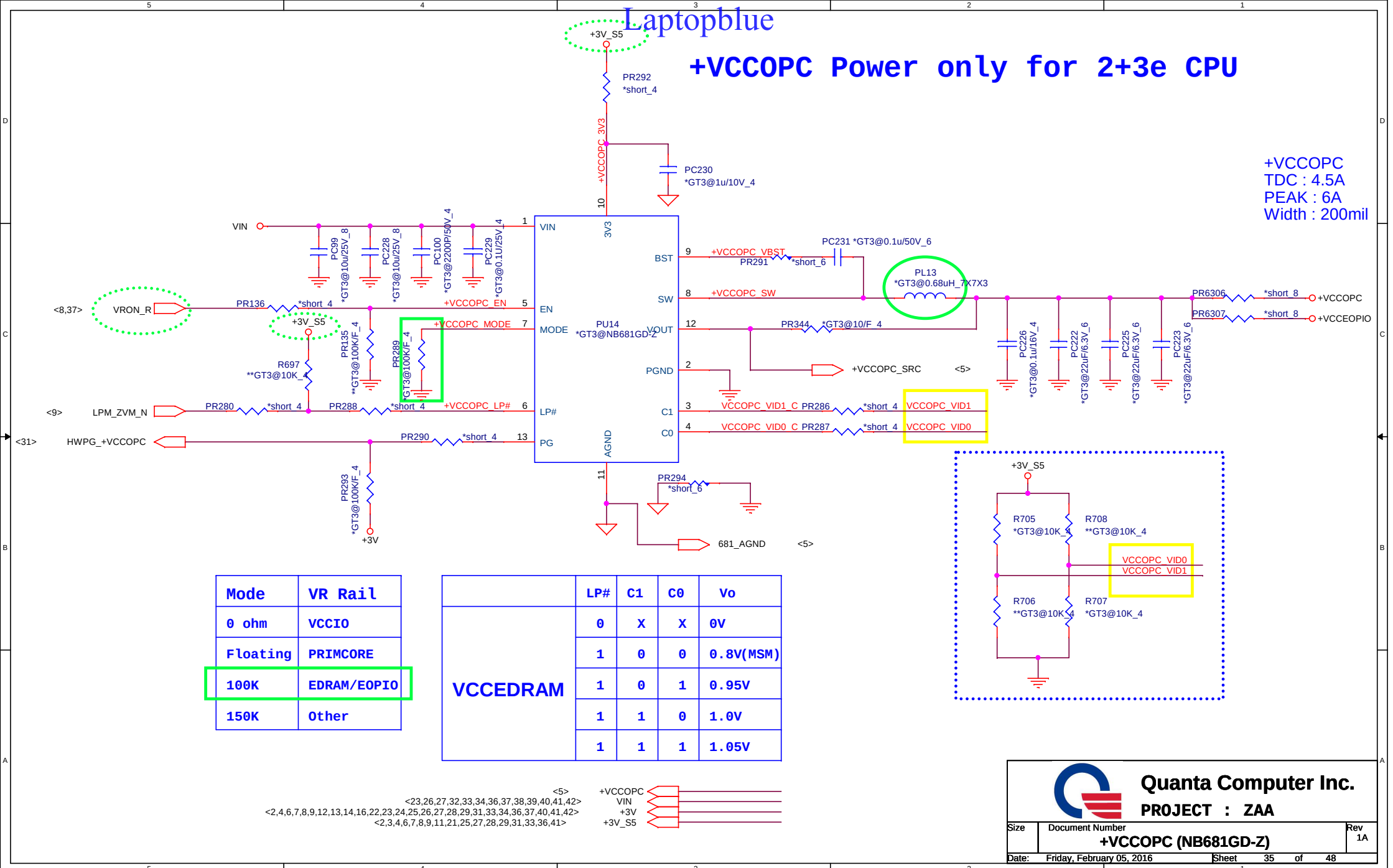
100

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+VCC0PC Power only for 2+3e CPU

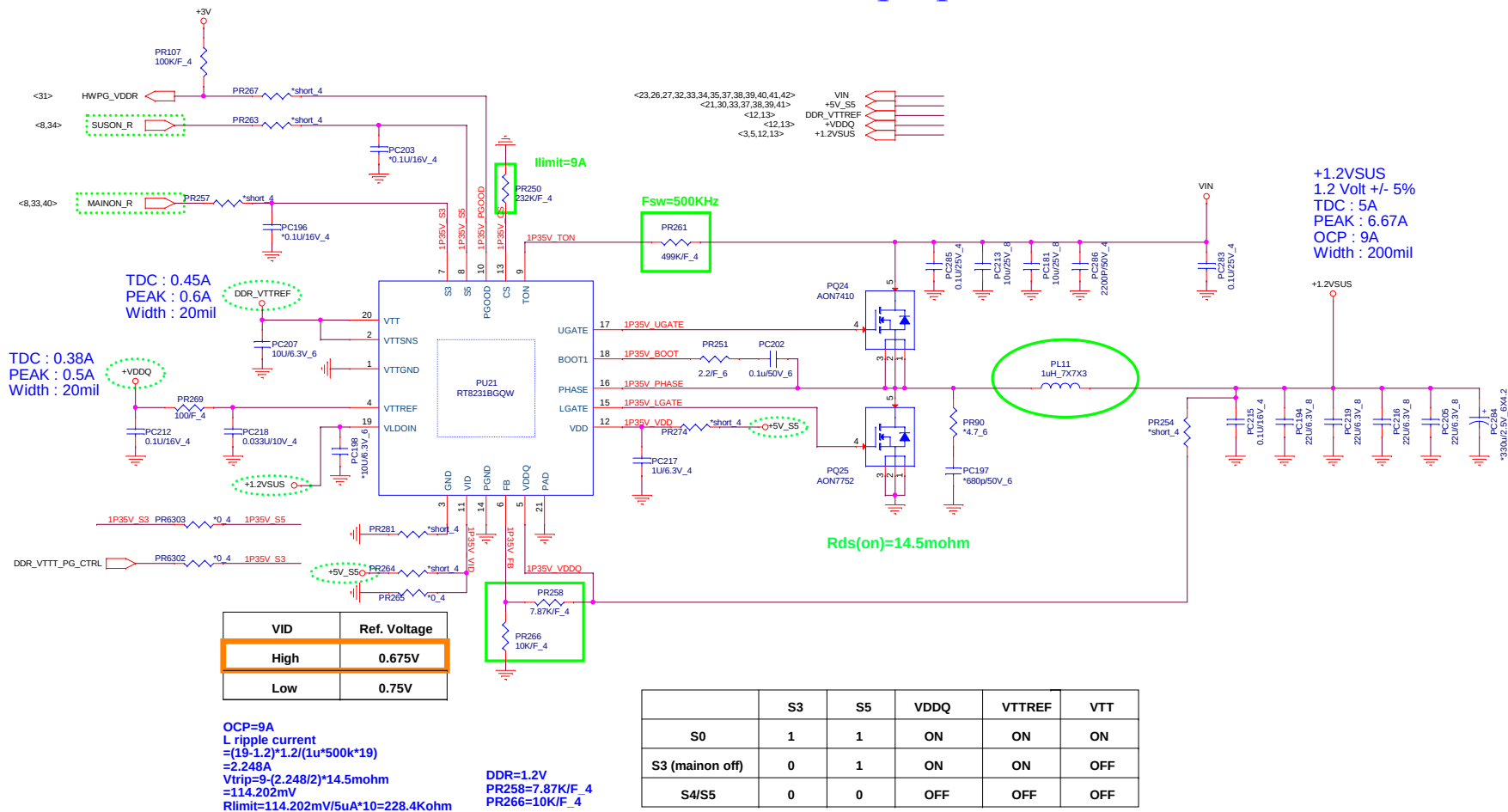
+VCCOPC
TDC : 4.5A
PEAK : 6A
Width : 200mil



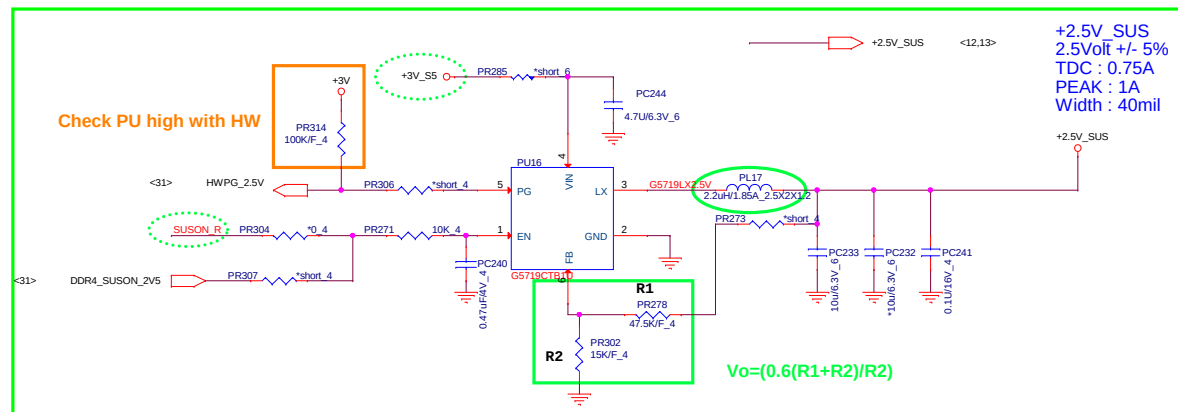
Mode	VR Rail
0 ohm	VCCIO
Floating	PRIMCORE
100K	EDRAM/EOPIO
150K	Other

	LP#	C1	C0	Vo
VCCEDRAM	0	X	X	0V
	1	0	0	0.8V(MSM
	1	0	1	0.95V
	1	1	0	1.0V
	1	1	1	1.05V

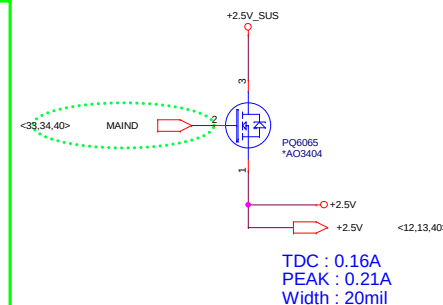
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+2.5VSUS Power Rail For DDR4



10/26 Reserve +2.5V for DDR4 VDDSPD

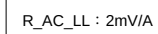


Check PU high with HW

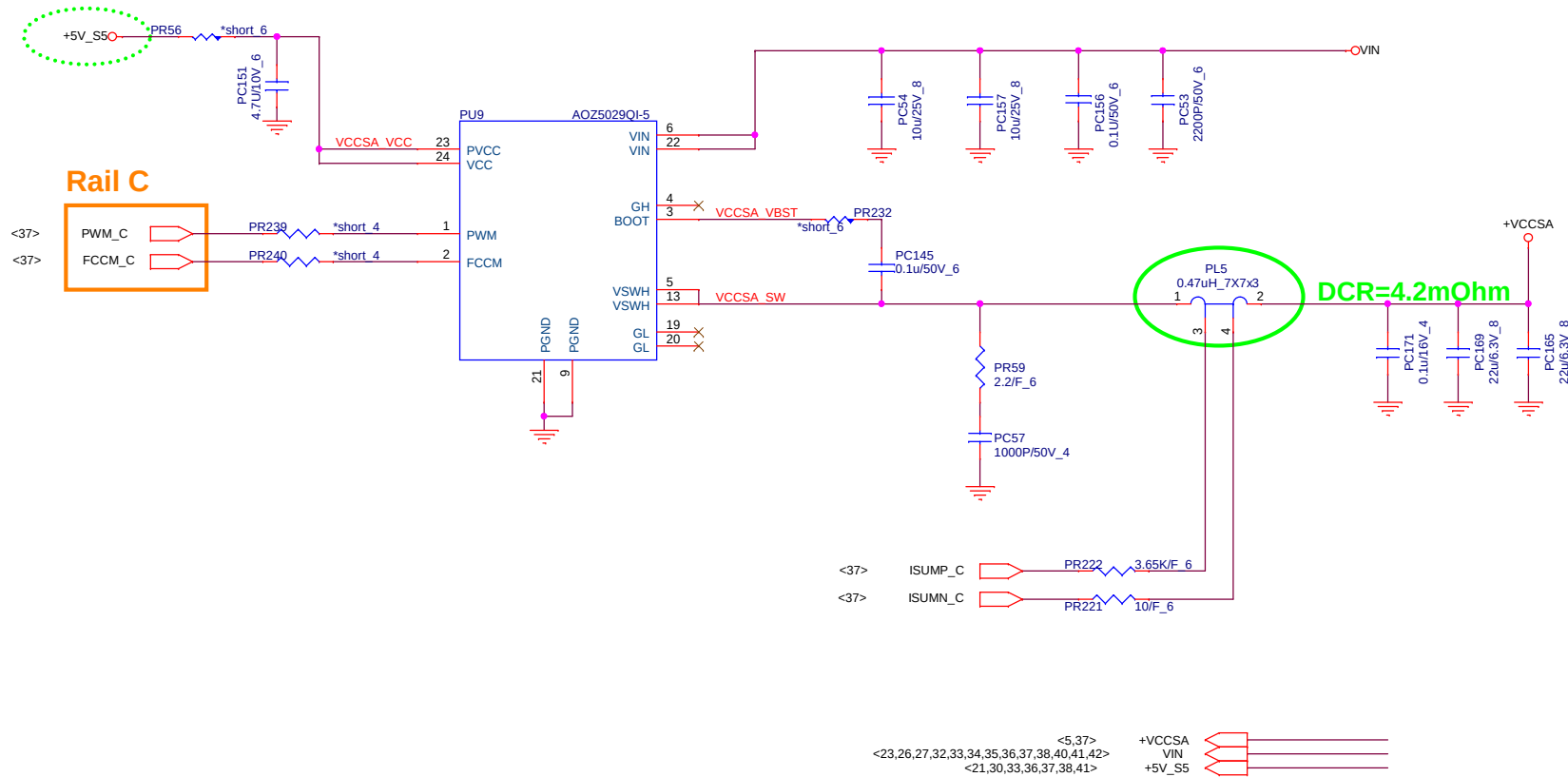


VCORE	VCCGT	VCCSA
Icc TDC PL2 : 23A	Icc TDC PL2 : 40A	Icc TDC PL2 : 5A
Icc Max : 29A	Icc Max : 64A	Icc Max : 5A
OCp : 35A	OCp : A	OCp : 6A
Fsw : 800KHz	Fsw : 800KHz	Fsw : 800KHz
VCORE L/L :	VCCGT L/L :	VCCSA L/L :
R_DC_LL : 2.1mV/A	R_DC_LL : 2mV/A	R_DC_LL : 10.3mV/A
R_AC_LL : 2.1mV/A	R_AC_LL : 2mV/A	R_AC_LL : 10.3mV/A

R_AC_LL : 2.1mV/A



VCCSA

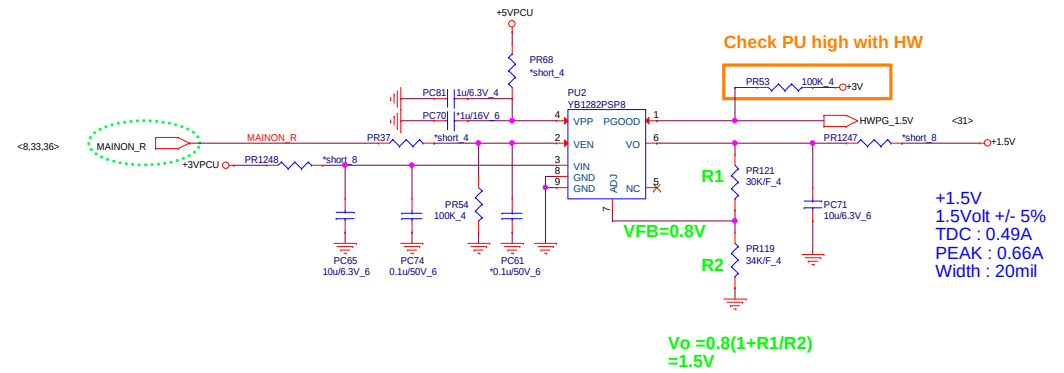
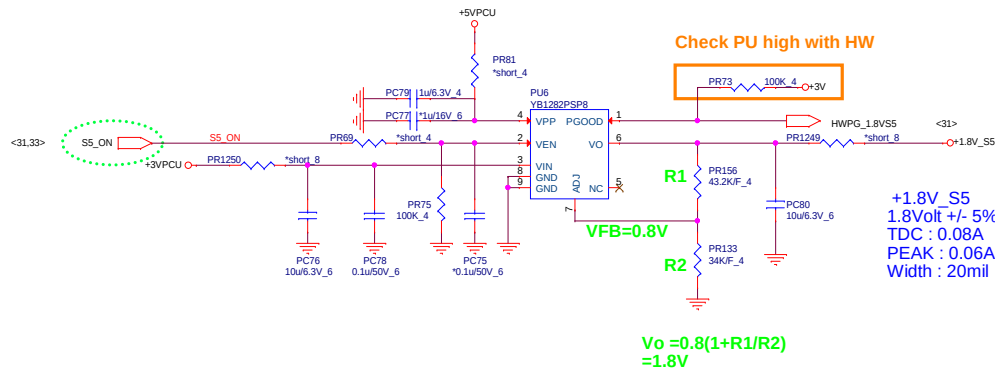


Quanta Computer Inc.
PROJECT : ZAA

Size	Document Number	Rev
	VCCSA (ISL95808HRZ-T)	1A

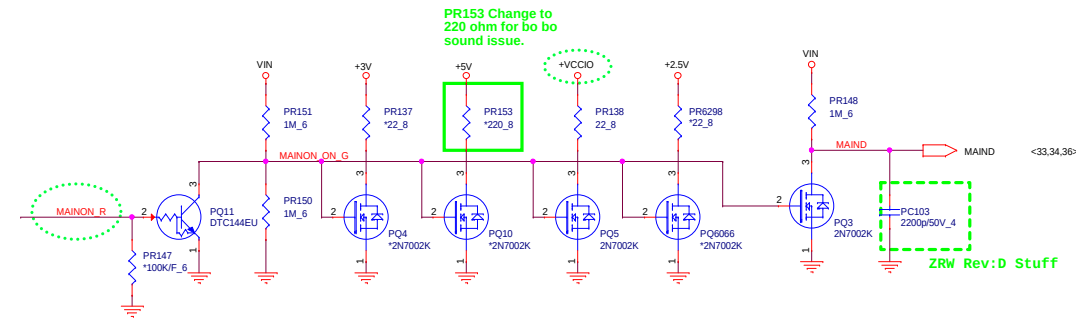
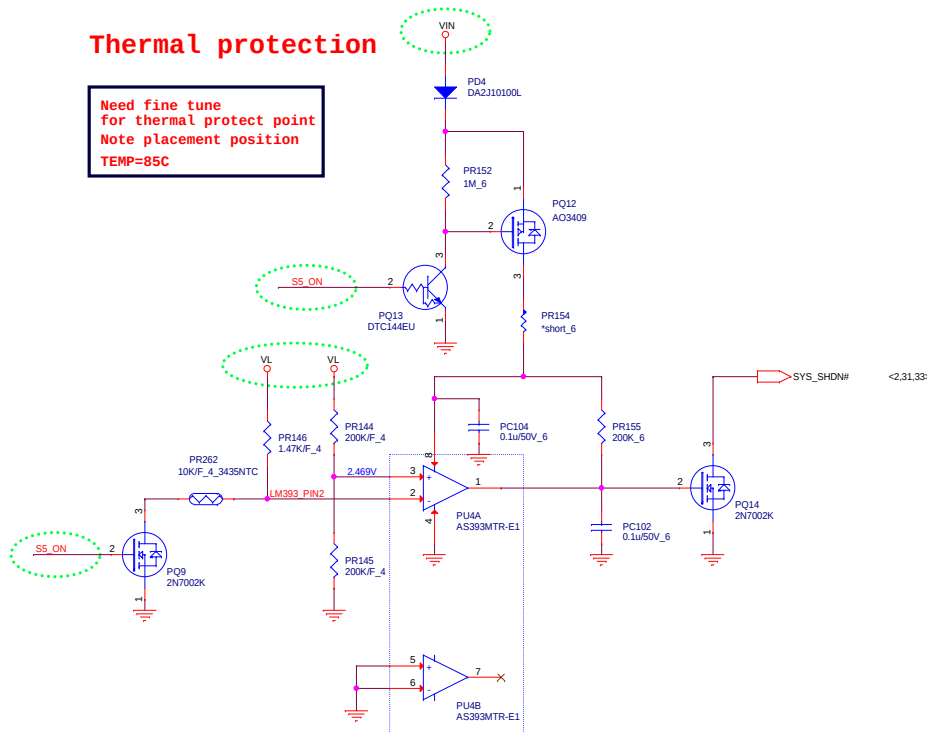
Date: Friday, February 05, 2016 Sheet 39 of 48

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Thermal protection

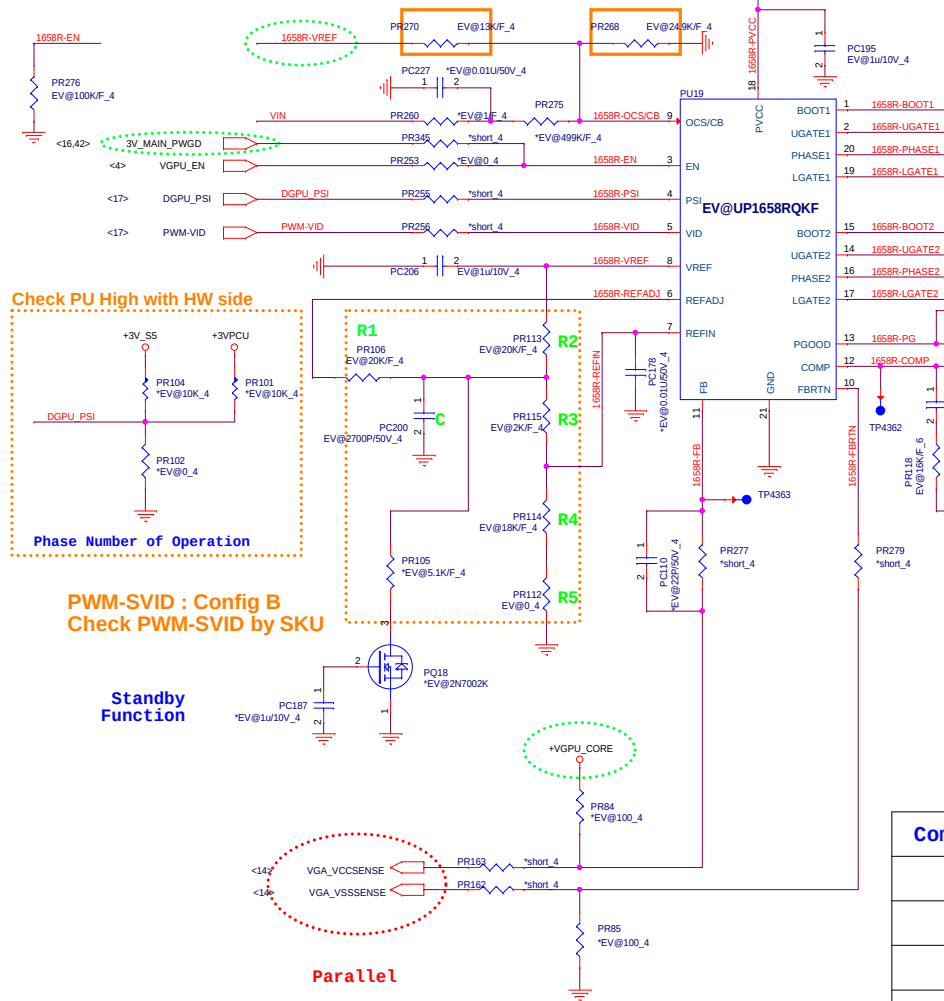
Need fine tune
for thermal protect point
Note placement position
TEMP=85C



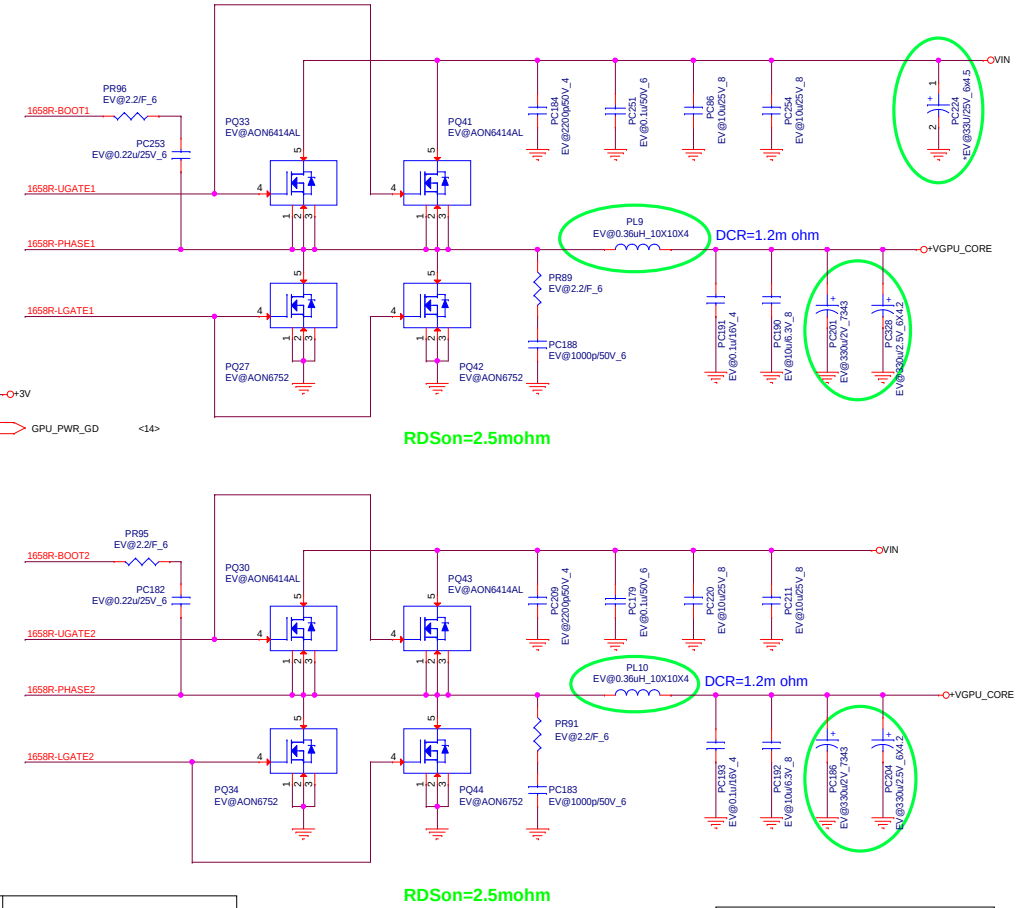
Quanta Computer Inc.
PROJECT : ZAA

Size	Document Number	Rev
	+1.8V/+1.5V/Thermal Protect	1A
Date:	Friday, February 05, 2016	Sheet 40 of 48

Double Check OCP SETTING



Component Value	Config B
R1	20K
R2	20K
R3	2K
R4	18K
R5	0 - ohm
C	2.7nF



N16P-GX(40W/GDDR5)
OpenVR Config:B

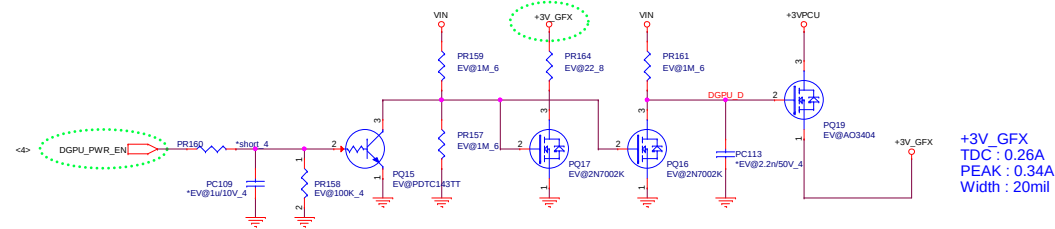
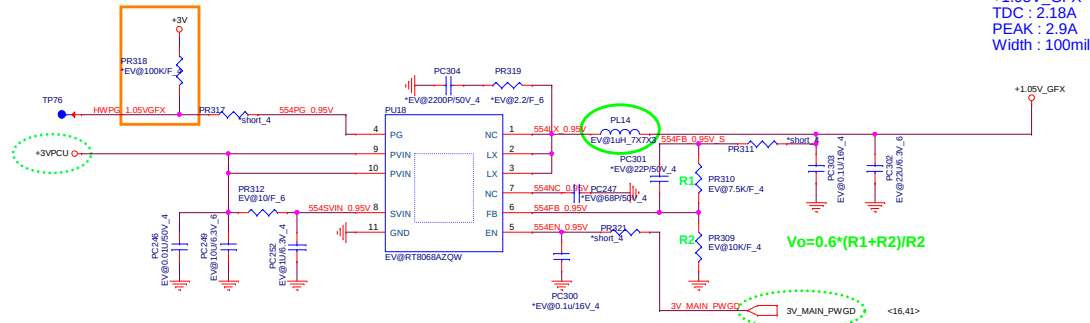
+VGPU_CORE
Continue current:51.1A
Peak current:87A
OCP:112A
FSW:300KHz
L/L=0mV/A

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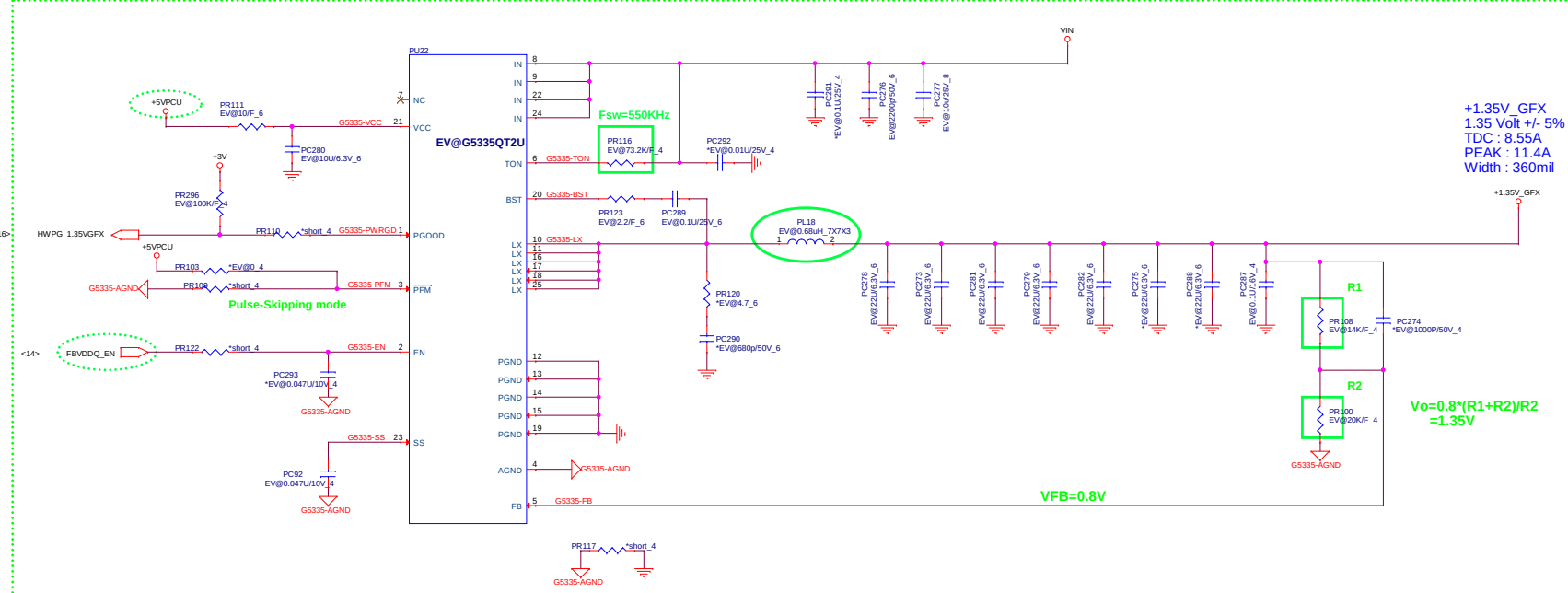
<14.15.16>
<14.16.17.31>
<15.19.20>

+1.05V_GFX
+3V_GFX
+1.35V_GFX

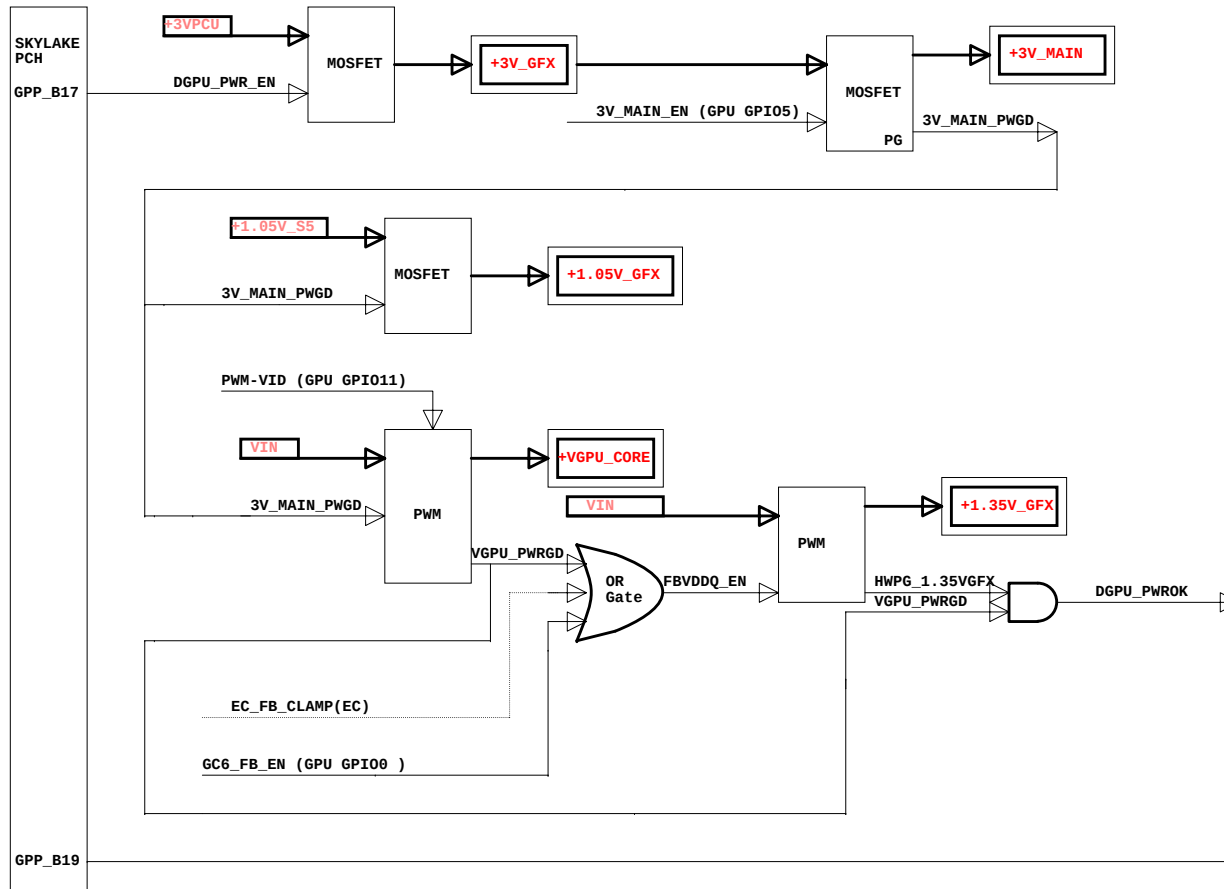
Check PU High with HW side



+1.35V_GFX for GDDR5

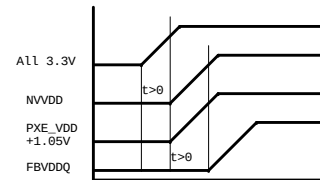
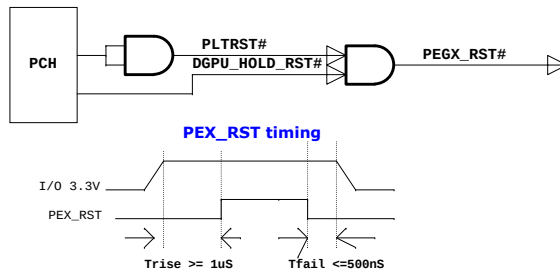


VGA power up sequence



Power plane	Description	Voltage	S0	S3	S5
+VCCCORE	Core voltage for CPU	0.55~1.5	ON	OFF	OFF
+VCCGT	Voltage for on-Die VGA of CPU	0.55~1.5	ON	OFF	OFF
+VCCGTX	Voltage for on-Die VGA of CPU	0.55~1.5	ON	OFF	OFF
+VDDQ_VTT	0.6V switched power rail for DDR4 terminator	0.6	ON	ON	OFF
+VDDQ	0.6V switched power rail for DDR4	0.6	ON	ON	OFF
+VCCSA	Voltage for system agent of CPU	0.55~1.15	ON	OFF	OFF
+1.2VSUS	1.2V switched power rail for DDR4	1.2	ON	ON	OFF
+1V_S5	1V switched power rail	1	ON	ON	ON
+1V_SUS	1V switched power rail	1	ON	ON	OFF
+VCCIO	Voltage for I/O of CPU	1	ON	OFF	OFF
+VCCOPC	Voltage for on package cache of CPU	1	ON	OFF	OFF
+2.5V_SUS	2.5V switched power rail for DDR4	2.5	ON	ON	OFF
+1.8V_S5	1.8V switched power rail	1.8	ON	ON	ON
+1.5V	1.5V switched power rail	1.5	ON	OFF	OFF
+3V_S5	3.3V switched power rail	3.3	ON	ON	ON
+3VPCU	3.3V always on power rail	3.3	ON	ON	ON
+3V	3.3V switched power rail	3.3	ON	OFF	OFF
+5VPCU	5V always on power rail	5	ON	ON	ON
+5V_S5	5V switched power rail for system	5	ON	ON	ON
+5V	5V switched power rail	5	ON	OFF	OFF
VIN	Adaptor power supply	19	ON	ON	ON
+2.5V	2.5V switched power rail for DDR4	2.5	ON	OFF	OFF
+3V_RTC	RTC power	3.3	ON	ON	ON
+VGPU_CORE	VGA power	0.6~1.2	ON	OFF	OFF
+1.05V_GFX	VGA power	1.05	ON	OFF	OFF
+1.35V_GFX	VGA power	1.35	ON	OFF	OFF
+3V_GFX	VGA power	3.3	ON	OFF	OFF
+5V_S5_V2	5V for Type-C source power rail	5	ON	ON	ON
+TYPEC_VBUS	5V Type-C power rail	5	ON	ON	ON

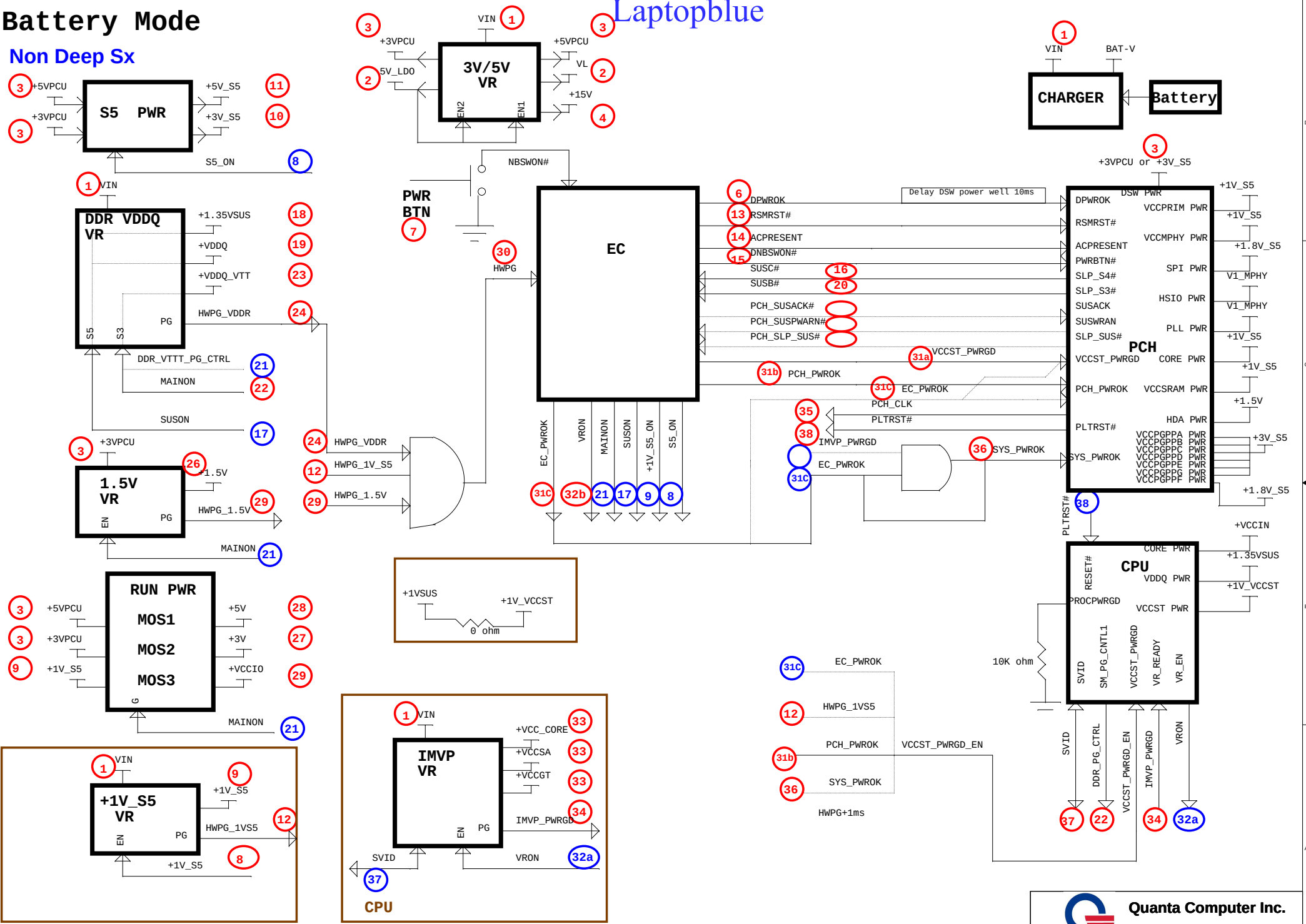
VGA Reset



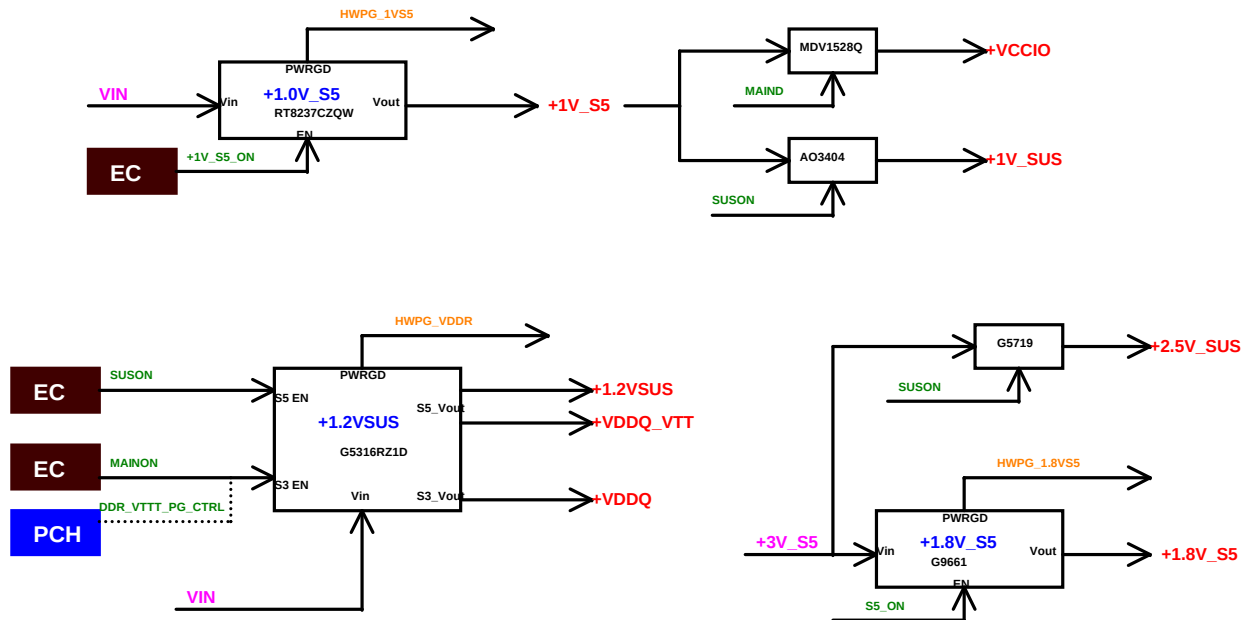
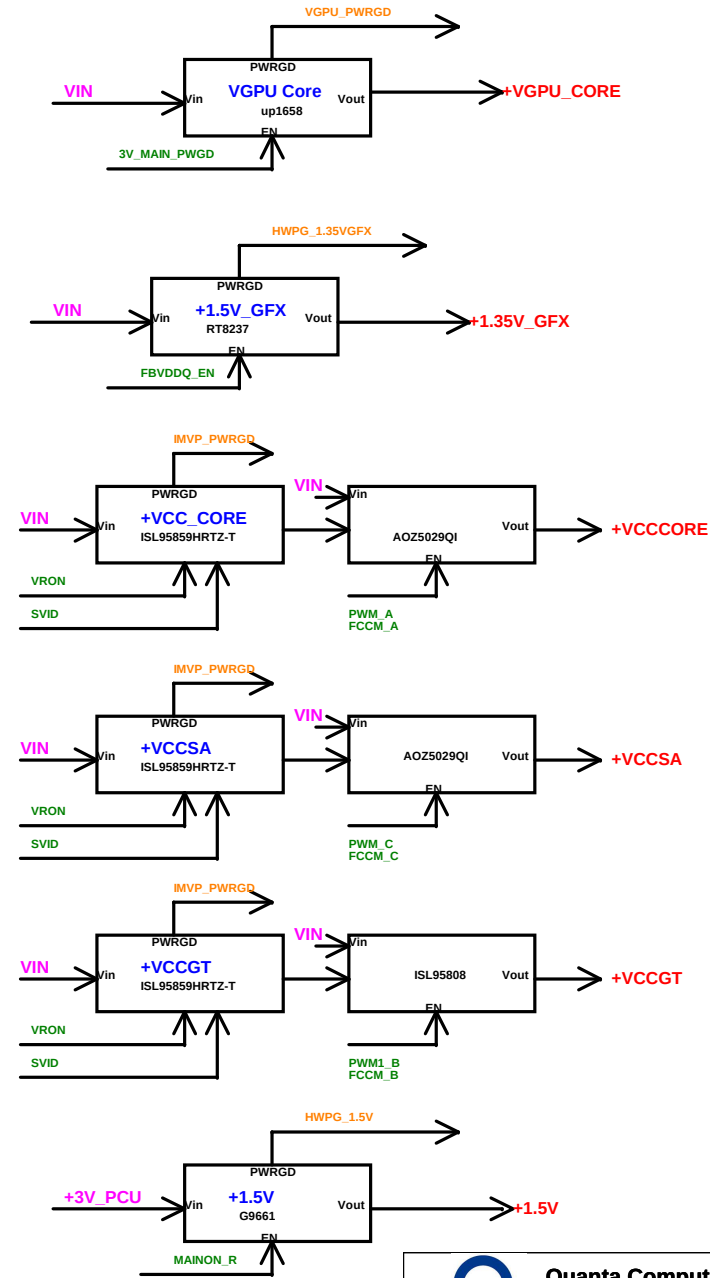
N15x Power on sequence
Notes: -All 3.3V includes all rails powered at 3.3V
-PEX_VDD 1.05V includes all rails that are shared

Battery Mode

Non Deep Sx

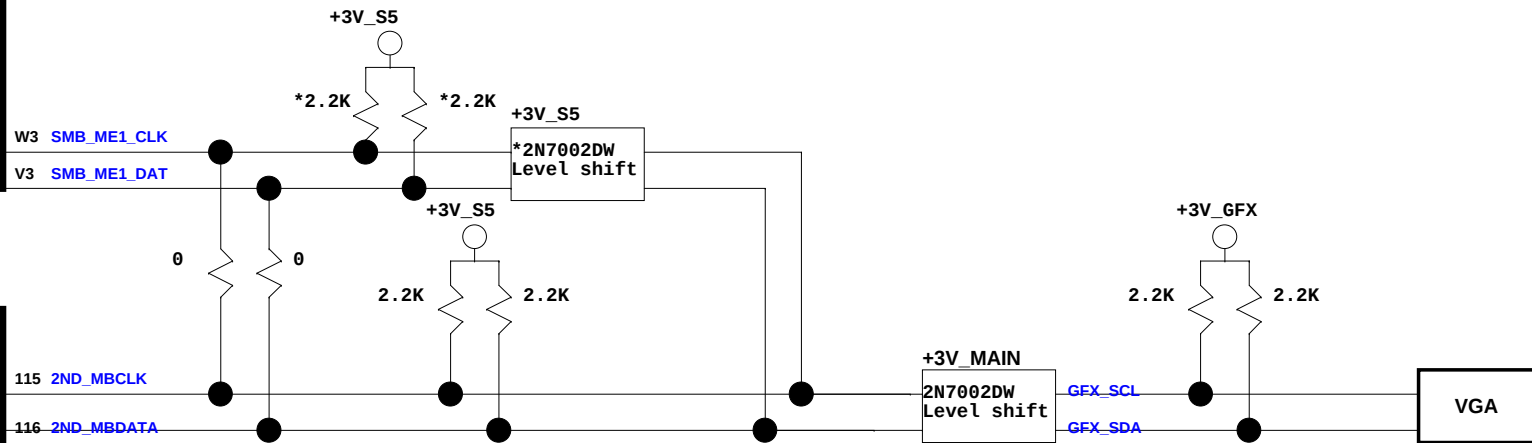
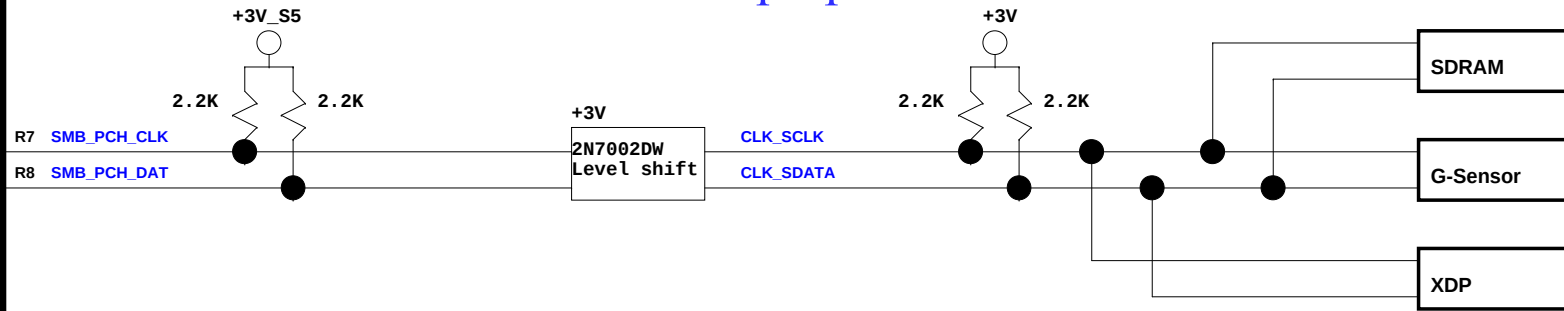


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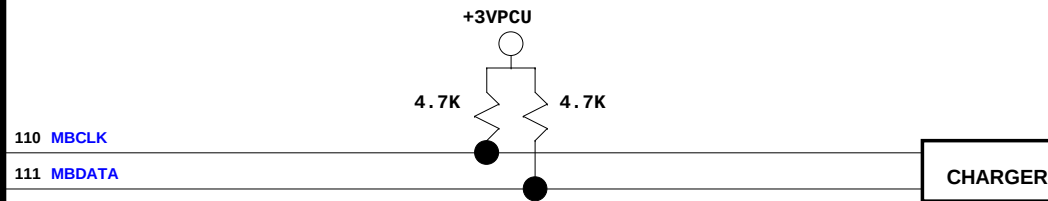


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Skylake U



EC
IT8987CX



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Model

Date

CHANGE LIST

B-CHANGE

B0. Change FP from 0201 to 0402; C689,C688,C683,C194,C241,C227,C216,C242,C205,C252 for RDC request.

B1. Change CN95, CN6, CN20,CN2019, CN7, JDIM1, JDIM2,CN10 of foot-print

B2. Page 33 Mount PR6296, remove PR6295 for EC can't boot issue

B3. Page 12 Delete R11170, mount R11133 for DDR4's SPD

B4. Page 13 Delete R11174, mount R11134 for DDR4's SPD

B5. Page 27 Change POA IC U1006's P/N. (AL000103006)

B6. Page 28 Change CN23's P/N--- 5H; Reserve R11284

B7. Page 25 change R247 value from 0 to 2.2 Ohm (CS-2204FA00); Change R251, R262, R269, R11265 footprint from 0603 to 0805 (LAN)--(CS07504FA11)

B8. Page 2 Mount R485 for THERMTRIP#

B9. Page 17 Change R4314 & R4306 of value for KA/KB

B10. Page 6 Mount Q6060 for CMOS issue

B11. Page 31 Swap U45 Pin81 & Pin32 for DAC Fan; Add D4015 for ESD; Reserve R11282 for battery

B12. Page 6 R512 Change P/N from 5% to 1 % (CS22702FB14)

B13. Page 8 IOAC setting change into none IOAC R598 mount , R599 remove.

B14. Page 29 Delete R328,R11109,R327,R347,R346,C4716,C4718,C4717,C4558 & Q6061; Add C321,C723,C728,C719,R218 & U12 for DAC Fan; Change CN8's P/N

B15. Page 29 Change KB/BL connector CN's FP,P/N. (DFFC04FR111) & remove CN2018 for ME request

B16. Page 29 Chage CP1-CP6 into 0402 size, from C4788-C4811

B17. Page 26 Change Speaker connector CN18's FP,P/N. (DFHD04MR176)

B18. Page 26 Modify U16,U4512 pin2 to +3V , then off U16 & U4512

B19. Page 15 Change C4117,C4118 from 22U into 10U, and Add C4815, C4812 (10U-0402) for layout speace.

B20. Page 18 Change C4423,C4426 from 22U into 10U, and Add C4813, C4814 (10U-0402) for layout speace.

B21. Page 31 Change SW4's P/N & FP; Add R1283 for EC AUTO RECOVERY.

B22. Page 28 Change Hole16's P/N & FP, Add Hole25, Hole26 for ME modify ; Add R11284

B23. Page 5 Change C202 value from 47U to 22U & add C4816

B24. Page 23 Change R11268,R11271 from 33 to 47 Ohm ; Change L5,L6,L7's P/N; Not mount C718,C716,C319,C333,C336

B25. Page 32 Change PJ3's FP

B26. Page 30 Change U22's FP

B27. Page 24 Change CN12's FP

B28. Page 4 Change C739 from 10 to 22P & mount for EMI request

B29. Page 21 Add C4817 & C4818 for EMI request

B30. Page 2 Change R577 & R152 power to +3V_S5 for leakage

B31. Page 8 Change R211 power to +3V_S5 for leakage

B32. Page 22 Add R11285, R11286(reserve)

B33. Page 21 Cancele co-layout R11225,R11226,R11227,R11228,R11229,R11230,R11231 & R11232.

B34. Page 14 Change C356 & 362 for vendor recommend

B35. Page 24 Mount R11277, Remove R11274 change to -4db

Power-CHANGE

B36. Page 33 Delete JP18, JP20 ,PR248,PR249,PR6127,PR6219,PR345,PR244,,PR247,PR246,PR266,PR272

B37. Page 34 Delete JP9

B38. Page 35 Delete JP16

B39. Page 36 Delete JP22,JP29

B40. Page 37 Change PR225,PR224's value from 10k to 13.7K; Add SP@ at PR194,PR203,PR207,PR202

B41. Page 38 Delete JP24, change JP25 to PR6304

B42. Page 39 Delete JP26

B43. Page 40 Delete PR6298,PQ6066,PR137,PQ4,PR153,PQ10; Change PU2 & PU6's P/N for ESD.

B44. Page 41 Delete JP34

B45. Page 42 Delete JP10,JP35

B46. Change DDR solution to RT8231B

Change +1V_S5 solution to G5335

Change +1.35V GFX solution to G5335

Revise LDO P/N to AL001282000 (YB1282PSP8)

LDO (PU2 & PU6) Pin4 adding 1u/6.3

B47. Page 37 Change PC10, PC20, PR192,PC28,PR211,PR220 & PC39 of value.

B48. Page 25 Add R6308

C-CHANGE

C1. Change 0 Ohm to short pad & remove JP,

R11, R14, R15, R28, R66, R67, R11129, R102, R194, R224, R229, R235, R790, R791, R792, R11111, R11112, R11113, R11140, R112, R135, R179, R180, R182, R185, R187, R188, R192, R193, R198, R240, R252, R11131, R164, R246, R339, R350, R11185, R11186, R550, R657, R718, R721, R782, R11153, R11283, R795, R796, R797, R816, R817, R818, R819, R820, R821, R11196, R11199, R11202, R11207, R11279, R11280, R11281, R948, R951, R956, R958, R959, R960, R11061, R11062, R11110, R11133, R11134, R11136, R11137, R11138, R11139, R11141, R11253, R11254, R11255, R11256, R11267, R11270, PR257, PR263, PR267, PR274, PR281, PR82, PR83, PR94.

PR87, PR254, PR264, PR109, PR110, PR117, PR122, JP8, JP10, JP14, JP15, JP17, JP22, JP33, JP19, JP21

R4328, R4335, R2855, R2870, R318, R221, R403, R405, R742, R743, R725, R745, L19, R2872

C2. Page 31 remove SW2 -- power bottom

C3. Page 29 Change CN20 & CN2019 K/B connector of P/N

C4. Page 27 Delete Q76, R11288; Add C4819, R11290 , R11291, R11298, R11299, R11302, R11303, R11300, R11301, R11292, R11293, R11294, R11295 for co-layout POA & PBA ; Reseeve EC52,EC53,R11289 & R11287

C5. Page 21 remove R11193, double mount at type-C

C6. Page 32 for power request change short pad to 10 Ohm, location PR209 & PR210; Change PC115 of value

C7. Page 8 remove R618, it can't mount, because none device.

C8. Page 38 mount PC138 -- power request.

012, 021, PR132

 Quanta Computer Inc. PROJECT : ZAA Change list Doc No Doc No Doc No Doc No	DOC NO.	PROJECT MODEL :	ZWA	APPROVED BY:		DATE:
		PART NUMBER:		DRAWING BY:		REVISION: